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| **ANIL KUMAR CHIDRA** | **C:\Users\Vijay\Downloads\62.jpg** |
| **Qualification : M.Tech (VLSI SYSTEM DESIGN)**  |
| **Experience: 12 Years** |
| **Area of Interest: Low Power VLSI, Digital IC design** |
| **Subjects Taught:*****UG Level:***1. Switching Theory and Logic Design
2. Computer Organization
3. Digital Logic Design
4. Digital IC Applications
5. Signals and Systems
6. Electronic Circuit Analysis
7. VLSI design
8. Probability and Stochastic Process
9. Digital Design Using Verilog HDL

**PG Level:**1**.** VLSI Technology –M.Tech ( VLSI&DSCE) 2. LOWPOWER VLSI DESIGN – M.Tech ( VLSI & DSCE) 3. Algorithms for Vlsi Design and Automation (VLSI). 4. CMOS Mixed IC Design. |
| **Research Publications:**1. CH.ANILKUMAR, M.DEVADAS, M.SWATHI **“A NOVEL LOW VOLTAGE CMOS CURRENT FEEDBACK AMPLIFIER”** in INTERNATIONAL JOURNAL OF ELECTRONICS AND ELECTRICAL ENGINEERING. ISSN:0974-2174.
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| **No of Projects guided:**

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| **UG** | **PG** |
| **10** | **6** |

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| **Workshops/Seminars/FDP’s Organized:*** National Level Workshop on **“ PCB Design and Fabrication”** on 30th March 2017.
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| **Workshops/Seminars/FDP’s Attended:**1. National level Workshop on “**LOW POWER VLSI DESIGN USING CADENCE TOOLS”** in VIT UNIVERSITY Chennai from JANUARY 24-25, 2013.
2. Two-Week ISTE Main Workshop on **“Analog Electronics”** Under the National Mission on Education through ICT (MHRD, Govt. of India) Conducted by IIIT Kharagpur at Prasad Engineering College Jangaon from 4th June- 14th June, 2013.
3. Two-Week AICTE Sponsored Faculty Development Program on **“Wireless Communication Technologies”** Organized by Dept of ECE Jayamukhi Institue of Technical Sciences Narasampet Warangal from 18th to 30th 2013.
4. Two-Week ISTE Main Workshop on **“Signals and Systems”** Under the National Mission on Education through ICT (MHRD, Govt. of India) Conducted by IIIT Kharagpur at SVS Group of Institutions, Warangal from 2nd Jan- 12th June, 2014.
5. Two Week Faculty Development (FDP) on **“ASPECTS OF IC DESIGN”** Organized by Electronics & ICT ACADEMY NIT WARANGAL, From 08.02.2016 to 17.02.2016 at NIT WARANGAL.
6. Twoday Facuty Development Program on **“ANALOG CMOS IC DESIGN”** from 28/04/2018 to 29/04/2018 in VIT University VELLORE.
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| **Professional Bodies:**1. Life Member of ISTE
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| **Achievements:**1. Ratified by JNTU Hyderabad.
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