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| KONREDDY THIRUPATHI | **C:\Users\User_01\Desktop\TH.png** |
| **Qualification : M TECH**  |
| **Experience: 10 years** |
| **Area of Interest: Communication Systems** |
| **Subjects** * Linear digital integrated circuits.
* Switching theory and logic design
* Control systems
* Pulse and Digital Circuits.
* Digital Signal Processing
* Digital logic design
* Voice over internet protocol
* Signals and Systems.
* Ad-hoc wireless sensor networks
* Digital logic design&computer organisation
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| **Research Publications:** 1. participated in the International journal of innovative Research in Technology paper title is LOW

COMPLEXITY WAVELET BASED CHANNEL ESTIMATIO WITH LOW LEAKAGE FOR OFDM SYSTEMS publication in e-journal . Volume-3 Issue-8 January 20171. participated in International journal for Innovative Engineering and management Research and the paper entitled Implementation of Dual Modulus Prescalar in True Single Phase Clock(TSPC) in the organizing committee of the Global publication Volume-01 Issue-02 November 2016
2. participated in International journal of electrical electronics and communication ISSN-2048- 1069,paper title is Different selection rules approach for interference cancellation in MIMO Volume:08 Issue:17 Dec-2014
3. participated in the international journal of VLSIsystem design communication systems paper title is 32- bit unsigned multiplier designed by CSLA,CLAA,CBLA adders, Organising committee SEMER GROUPS at hyderabad india during November 2014 SG:IJVDCSV02IS10P3343-2
4. participated in the International journal of Professional Engineering Studies(IJPRES) paper title is An sui channel based multi user interference suppression for UWB system Volume-5 Issue-2 July 2015
5. participated in International conference on electronics communications and VLSI circuits(ICECV-2015) paper title is Proposed encoding Scheme for Reduction energy consumption in network on chip for conference publication.
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| **UG** | **PG** |
| **11** | **7** |

**No of Projects guided:** |
| **Workshops/Seminars/FDP’s Attended:**1. work shop on SDP hands on digital signal processing tools algorithms and architectures conducted by jayamukhi institute of technological sciences narsampet Warangal 7thto 19th December 2009.
2. one week work shop on VLSI & embedded systems conducted by vaagdevi engineering college, during 13th to 20th September 2011.
3. participated in two week work shop on computer programming conducted by Indian institute of technology Bombay from May 20th 2014 to june 21 st 2014
4. participated in work shop on DEFENCE ELECTRONICS organized by the department of electronics and communication engineering kakatiya university college of engineering & technology on 5th February 2014
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| **Achievements:** **1)** Qualified in Faculty eligibility test FET- 2011 JNTU Hyderabad 2) I got 8th rank in PG-SET 2007, which is conducted by JNTUH |