|  |  |
| --- | --- |
| **MATTA DEVADAS** | **C:\Users\Vijay\Downloads\pic.jpg** |
| **Qualification : M.E ( Ph.D - JNTU ANANTHAPURAMU )** | |
| **Experience: 09 Years** | |
| **Area of Interest: Low Power Vlsi, System On Chip, Digital IC design** | |
| **Subjects Taught:**  ***UG Level:***   1. VLSI design 2. Computer organization 3. Digital logic design & Computer Organization 4. Optical communications 5. Integrated Circuits and Applications 6. Digital Logic Design 7. Nano Technology 8. Microprocessors and Interfacing 9. Switching Theory and Logic Design 10. Digital Design Using Verilog HDL 11. Digital Logic Design and Microprocessors   **PG Level:**  1**.** VLSI Technology –M.Tech ( VLSI&DSCE)  2. System on chip Architecture – M.tech (VLSI)  3. CPLD & FPGA Architecture and Applications – M.Tech (VLSI &DSCE)  4. LOWPOWER VLSI DESIGN – M.Tech ( VLSI & DSCE)  5. Algorithms for Vlsi Design and Automation (VLSI).  6. ASIC Design. | |
| **Research Publications:**   1. M DEVADAS, RANA SIDDIQUA **“A HIGH SPEED MODIFIED DESIGN OF EFFECTIVE SIGN DETECTION ALGORITHM FOR RESIDUE NUMBER SYSTEM”** in INTERNATIONAL JOURNAL OF VLSI SYSTEM DESIGN AND COMMUNICATION SYSTEMS” IJVDCS2015 Vol 03, Issue 04 July 2015. ISSN 2322-0929. 2. M DEVADAS, CHANDANA.P **“A NOVEL DESIGN OF 32 BIT UNSIGNED MULTIPLIER USING MODIFIED CSLA”** in INTERNATIONAL JOURNAL OF RESEARCH IN ADVENT TECHNOLOGY. Vol 03, No 07, July 2015. E-Issn: 2321-9637. 3. M DEVADAS LAVANYA A.**“MIXED SIGNAL IMPLEMENTATION OF CARRY SELECT ADDERS FOR LOW POWER APPLICATIONS”** IN INTERNATIONAL JOURNAL OF COMPUTER SCIENCE INFORMATION AND ENGG.. TECHNOLOGIES” IJCSIET 2014. ISSN NO: 2277-4408. 4. M.DEVADAS, G.LAKSHMI. **“MODELING AND SIMULATION OF 1 BIT LOW POWER FULL ADDER USING FINFET”** IN IOJETR JOUNAL VOL 8 OCTOBER 2014. 5. M DEVADAS, HUBERT GEORGE **“IMPLEMENTATION OF MULTIUSER MIMO SYSTEM USING QUANTIZED CSI BASED TOMLINSON-HARSHIMA PRECODING”** IN INTERNATIONAL JOURNAL OF SCIENTIFIC ENGINEERING AND TECHNOLOGY RESEARCH (IJSETR 2014). ISSN NO:2319-8885. 6. m devadas, g vedavathi **“a novel implementation of weighted 2n +1 adder wit simple correction schemes”** IN INTERNATIONAL CONFERENCE ON ADVANCES IN ELECTRICAL,ELECTRONICS,MECHANICAL AND COMPUTER SCIENCE ON 22nd September 2013. 7. M DEVADAS, B RAMPRASAD **“ DESIGN OF CASCADED ANALOG-TO-DIGITAL CONVERTER BY USING VOLTAGE CONTROLLED OSCILLATOR**” in INTERNATIONAL ACADEMIC CONFERENCE ON ELECTRICAL, ELECTRONICS AND COMPUTER ENGINEERING on 22nd OCTOBER 2013. 8. M DEVADAS, B VIJAY KUMAR G MADHURI CH ANILKUMAR **“Mobile Controlled Handoff by using Dyanamic Channel Assignement”** in ieee, International Multi Conference on Automation, Computing, Control, Communication and  Compressed Sensing, iMac4s-2013 on 22-23rd March 2013 Kerala India.   IEEE Catalog Number CFP1341U-DVD ISBN Number 978-1-4673-5088-4   1. M.DEVADAS, M.SWATHI, CH.ANILKUMAR **“A NOVEL LOW VOLTAGE CMOS CURRENT FEEDBACK AMPLIFIER”** in INTERNATIONAL JOURNAL OF ELECTRONICS AND ELECTRICAL ENGINEERING. ISSN:0974-2174. 2. M.DEVADAS, K.SOUMYA **“ZERO PADDED SYMMETRIC CONJUGATE SELF CANCELLATION TECHNIQUE IN MB-OFDM SYSTEM DESIGN”** in INTERNATIONAL CONFERENCE ON ADVACNES IN ELCETRICAL ELECTRONICS & COMPUTER SCIENCE. ISBN: 978-93-81693-88-4. 3. M.DEVADAS, B.ANITHA **“FULL PROTECTION TECHNIQUE TO IMPROVE REGISTER FILE IMMUNITY AGAINST SOFT ERRORS”** In INTERNATIONAL CONFERENCE ON ELECTRICAL,ELECTRONICS AND COMPUTER SCIENCE,by IRD INDIA.ISBN:978-93-81693-68-6. 4. M.DEVADAS,K LATHA **“Design of High performance On-Chip bus OCP-IP Protocol with Advanced Bus Functionalities”** in International Journal of Advances in Electronics Engineering. Vol:1 Issue:1 ISSN 2278 - 215X 5. M.Devadas,M.Sanajy,Ch.Pavan kumar,P.Srujan **“A NOVEL APPROACH FOR FAULT TOLERANT NANOMEMORY APPLICATIONS”** in INTERNATIONAL CONFERENCE ON NANO SCIENCE,ENGINEERING & ADVANCED COMPUTING ICNEAC-2011” organized by IACQER. ISBN:978-81-8465-683-1. 6. M.DEVADAS, NILOFAR ANJUM **“A Gate-Block Selection Algorithm for extracting parameters of a Low-Power Pre-computation-Based Content-Addressable Memory”** in NATIONAL CONFERENCE ON SIGNAL PROCESSING AND EMBEDDED SYSTEMS APPLICATIONS (SPESA-2011)”Sponsored by AICTE& DRDO.ISBN:978-93-81075-46-3. 7. M.DEVADAS, M.SANJAY,LAVANYA **“Reduction of Power Dissipation using Twin Precision Technique and the Implementation of Baugh–wooley Algorithm”** in *International Conference on* Technology and Management(ICTM–2011) organised by IRDO.ISBN:978-93-81361-08-5. 8. M DEVADAS, K.LATHA **“DESIGN OF HIGH PERFORMANCE ON-CHIP BUS INTERFACE”** in NATIONAL CONFERENCE ON SIGNAL PROCESSING AND EMBEDDED SYSTEMS APPLICATIONS (SPESA-2011)”Sponsored by AICTE& DRDO.ISBN:978-93-81075-46-3. 9. M.DEVADAS,M.SWETHA,M.SANJAY **“DESIGN TOPOLOGIES FOR LOWPOWER FULL ADDER”** in 4th NATIONAL CONFERENCE and ISTE STATE CHAPTER ANNUAL CONVENTION On Wireless communication & VLSI Design (NCWCVD-2011). 10. M.Devadas, P.karthigai kumar **“AN EFFICIENT FPGA IMPLEMENTATION OF IDEA CRYPTOGRAPHIC ALGORITHM”** in NATIONAL CONFERENCE ON COMMUNICATION NETWORKS” in Thrissur, Kerala. 11. M Devadas,Saritha **“DESIGN AND IMPLEMENTAION OF PIPELINED ANALOG TO DIGITAL CONVERTER”** In NATIONAL CONFERENCE ON RECENT ADVANCEMENTS IN COMMUNICATION & ELECTRONICS” RACE’11. 12. M.Devadas,Mahitha**“LOW POWER HIGH SPEED MULYI THRESHOLD VOLTAGE INTERFACING CIRCUITS AND ITS APPLICATION”** In 2010 NATIONAL CONFERENCE ON ELECTRONICS AND COMMUNICATION. | |
| |  |  | | --- | --- | | **UG** | **PG** | | **16** | **14** |   **No of Projects guided:** | |
| **Workshops/Seminars/FDP’s Organized:**   * **National Level Technical and Cultutal Fest SAPIENTIA** 2K11, March17th -18th , 2011. * **National Level Robotic Workshop**,March 9th and 11th 2013. * **2nd  National Level Technical and Cultutal Fest SAPIENTIA 2K13,** March 15th - 16th, 2013. * **National Level Robotic Workshop** on March 11th and 12th 2014. * **National Level Technical and Cultutal Fest TECHNOCRAFT 2K14 on** March 14th ,15th and 16th 2014. * **National Level Technical and Cultutal Fest TECHNOCRAFT 2K14 on** March 14th ,15th and 16th 2014. * **“HANDS ON METOR GRAPHICS an EDA Tool”** A two day Natioal Level Workshop on September 30th and October 1st 2016. * A Two Day National Level Workshop on **“ RASPBERRY Pi and Internet of Things”** on 16th and 17th October 2017. | |
| **Workshops/Seminars/FDP’s Attended:**   1. Workshop on **“VLSI DESIGN METHODOLOGIES BY USING MENTOR GRAPHICS DESIGN TOOLS”** in JNTUH HYDERABAD 8th-13th Aug 2010. 2. One day Tutorial on **“TRANSMISSION LINES,ANTENNAS AND MICROWAVE ENGINEERING”** by IEEE HYD Section in SR Engg College Warangal 26th FEB 2011. 3. One day Tutorial on **“WEB SERICES:ARCHITECTURE,DESIGN AND DEVELOPMENT”** by IEEE HYD Section in SR Engg College Warangal 5th march 2011. 4. Workshop on **“Trends in VLSI Design & Mentor Graphics Tool-TVDM-11”** in Guru Nayak Dev Engineering College,Bidar from 12th-14th May 2011. 5. National level Workshop on “**LOW POWER VLSI DESIGN USING CADENCE TOOLS”** in VIT UNIVERSITY Chennai from JANUARY 24-25, 2013. 6. Two-Week ISTE Main Workshop on **“Analog Electronics”** Under the National Mission on Education through ICT (MHRD, Govt. of India) Conducted by IIIT Kharagpur at Prasad Engineering College Jangaon from 4th June- 14th June, 2013. 7. Two-Week AICTE Sponsored Faculty Development Program on **“Wireless Communication Technologies”** Organized by Dept of ECE Jayamukhi Institue of Technical Sciences Narasampet Warangal from 18th to 30th 2013. 8. National Workshop on **“Embedded Systems for Automation and Instrumentation”** Organized by the Centre for Automation and Instrumentation,National Institute of Technology Warangal Sponsored by TEQIP Phase-II during 12th-14th December 2013. 9. Two-Week ISTE Main Workshop on **“Signals and Systems”** Under the National Mission on Education through ICT (MHRD, Govt. of India) Conducted by IIIT Kharagpur at Prasad Engineering College Jangaon from 2nd Jan- 12th June, 2014. 10. One week **“Course work on Research Methodology”** in JNTU University Anathapuramu from 03rd – 08th Nov 2014. 11. A Two day National Workshop on **“RECENT ADVANCES IN VLSI”** Conducted by IETE and Dept of ECE in Kakatiya Institute of Technology and Science Warangal from 8th & 9th Nov 2014. 12. A One day National Level Workshop on **“Embedded Systems”** Conducted by Dept of EEE KU College of Engg and Technology Warangal on 7th Feb 2015. 13. A Two Day National Workshop **on “PROGRAMMBLE LOGIC CONTROLLERS AND SCADA PROGRAMMING (PLC-SCADA)”** Conducted by Department of Instrumentation & USIC Sri Krishnadevaraya University from 20th – 21st November 2015 at Sri Krishnadevaraya University Ananthapuramu. 14. One week Faculty Updation Program (FUP) on **“DIGITAL VLSI SYSTEM DESIGN USING VERILOG HDL”** organized by C-DAC, HYDERABAD in Collaboration with TASK from 18.01.2016 to 22.01.2016 at C-DAC HYDERABAD. 15. Two Week Faculty Development (FDP) on **“ASPECTS OF IC DESIGN”** Organized by Electronics & ICT ACADEMY NIT WARANGAL, From 08.02.2016 to 17.02.2016 at NIT WARANGAL. 16. A Two Day Workshop for University & College Teachers on **“SKILL BASED COURSES (SBC-2016)”** Organized by Centre for Skill Development Entrepreneurship and Incubation Sri Krishnadevaraya University from 21.03.2016-22.03.2016 at Sri Krishnadevaraya University Ananthapuramu. 17. One day National Level Workshop on **“OUTCOME BASED EDUCATION”** in JNTU Hyderabad on 19/10/2016. 18. A Twoday National Level Workshop on **“FREE &OPEN SOURCE SOFTWARES IN TEACHING & LEARNING”** from 04/03/2017-05/03/2017 NIT Warangal. 19. One day Faculty Knowledge Program on 11th august 2017 conducted by ICFAI Business School. 20. One day Facuty Development Program on **“Networking Simulation using Qualnet Software”** on 28th sept 2017 Conducted by Dellsoft Technologies. 21. One day Facuty Development Program **on “Circuit Simulation using Target 3001 software”** on 20th sept 2017 Conducted by Dellsoft Technologies. 22. Twoday Facuty Development Program on **“ANALOG CMOS IC DESIGN”** from 28/04/2018 to 29/04/2018 in VIT University VELLORE. | |
| **Professional Bodies:**   1. IEEE 2. IAENG | |
| **Achievements:**   1. Ratified by JNTU Hyderabad. 2. Qualified in Faculty Eligibility Test Conducted by JNTU Hyderabad. 3. Qualified in GATE. 4. Applied for Research Grants from AICTE. | |