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| **RAYABARAPUVENKATESWARLU** | **C:\Users\VCEW\Desktop\2.jpg** |
| **Qualification : M.TECH(DSCE) JNTU HYDERABAD** | |
| **Experience:**  I started my career as Lecturer in the year 2007 at RAMAPPA ENGINEERING college Warangal ,before this I worked as Asst professor in the dept of ECE at Sri rajarajeswari engg college Karepally ,Khammam for one year. Then I shifted to Warangal.I worked for long five years at RAMAPPA ENGINEERING college.To strengthen my career I shifted to VAAGDEVI COLLEGE OF ENGINEERING in the year 2013.I joined as Asst professor in the dept of ECE on 24-06-2013. | |
| **Area of Interest: VLSI DESIGN** | |
| **Subjects Taught:**  ECA, EDC,MPIF, MWE, OC, PDC, LDICA,VLSI TECHNOLOGY, EC,STLD,CMC,TSSN,STLD,WCN ,PDLIC and RADAR SYSTEMS for undergraduate (UG) students& Real Time Operating Systems for Embedded Systems,H/W S/W CoDesign,Wireless Networks | |
| * **Research Publications**:  1. Published a paper with title A Neural Network Approach to Pulse Radar on a Softcore Processor at International Journal Electronics and Computer Technology(IJECT)-Vol-II SP-1,Dec 2011 with paper id IJECT/1011/2SP . 2. Published a paper with title FPGA IMPLEMENTATION OF PARTIAL DISCHARGE DETECTION TO COUNT PD SIGNALS FOR HV APPLICATIONS at SCIEI-International Conference on Electrical , Electronics and Communication Engineering(SCIEI-IACEECE-2013)on 15,SEP 2013 at PUNE,INDIA. 3. A Novel 6T SRAM based design with integration of NBTI technique at International Conference on Electronics,Communications and VLSI Circuits July 2015 with issn no:2348-4845 4. Design and Implementation ofI2c Master Bus Controller using VHDL Language on 13-14 dec 2014 at International conference on Emerging Trends in Electronics and Communications. 5. **Soft core processor by neural network pulse compressor accomplishment at International Conference on Innovative Trends in Engineering and Management**(ICITEM-2017) (Page No: 3086-3089). | |
| **No of Projects guided:**   |  |  | | --- | --- | | **UG** | **PG** | | 24 | 12 | | |
| **Workshops/Seminars/FDP’s Organized:**   1. Conducted Two Week Adjunct course on PSPICE and MATLAB at **Ramappa** **Engg College** , Warangal in 2008. 2. Conducted Three Day Faculty Development Program on Embedded Systems at **Ramappa Engg College, Warangal** in 2011. 3. Conducted Two day workshop on Development of Android and its Applications at Vaagdevi College Of Engineering,Warangal in May 2014. 4. Conducted Two Week Adjunct course on PSPICE and MATLAB at **Ramappa** **Engg College** , Warangal in 2008. | |
| **Workshops/Seminars/FDP’s Attended:**   1. Attended Two Week Faculty Development program at **KITS,Warangal** on Hands on approach of OFDM using matlab in Nov –Dec 2017. 2. Attended Two Week Faculty Development Program at **NIT,Warangal** on DSP Processors in 2009. 3. Attended Two Week Faculty Development Program at **NIT, Warangal** on Electronic Circuit Analysis and Design in 2010. 4. Attended NPTEL Two week training programme at SVSIT ,Bheemaram,Warangal in May 2014 | |
| **Conferences Attended:**   1. ICITEM 2017 | |