Vedavathi Gonela

Qualification : M.Tech (VLSI System Design)

Experience: 07 Years

Area of Interest: Signal Processing & Embedded Systems

Subjects Taught: STLD,SS,DLD&MP, DLD&CO,DSP,RS & DSPA

Research Publications:

1. Published a Paper titled" Adaptive test Pattern genaration using BIST Schemes",International journal of reasearch(IJR),vol-2,Issue-12 December-2015.ISSN:2348-6848.

No of Projects guided:

UG	PG
10	01

Workshops/Seminars/FDP's Attended:

1. Attended workshop on "Signal processing for Communications" Organised by the Electronics&ICT Acadamy National Institute of Technology,warangal during 4th-8 th Jan 2016.
2. Attended workshop on "Electro magnetic Transmission lines" Organised by JNTU, Jagithyal in March-2013.

Conferences Attended:

1. Attended International Conferenceon Advances in electrical,Electronics,Mechanical and Computer Science and presented a paper entitled anovel implementation of "weighted modulo 2^n+1 adder with simple correction schemes held on 22nd september-2013 at hyderabad.