COURSE STRUCTURE AND
DETAILED SYLLABUS

M.TECH
VLSI SYSTEM DESIGN

For
M.TECH TWO YEAR DEGREE PROGRAMME
(Applicable for the batches admitted from 2018-2019)

VAAGDEVI COLLEGE OF ENGINEERING
(Autonomous)
Bollikunta, Warangal-506 005
Telangana State, India.
# M.Tech-VLSI System Design

## R18 Regulations

### VAAGDEVI COLLEGE OF ENGINEERING

Autonomous  
Bollikunta, Warangal

### Department of Electronics & Communication Engineering

**M.TECH. (VLSI System Design)**

**COURSE STRUCTURE**

(R18 Regulations applicable for the batches admitted from Academic Year 2018-19 onwards)

### I-SEMESTER

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**Total Credits** 16 00 08 18

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**Total Credits** 14 00 12 18

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*Department of ECE* 

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VAAGDEVI COLLEGE OF ENGINEERING  
Autonomous  
Bollikunta, Warangal  

Department of Electronics & Communication Engineering  
M.TECH. (VLSI System Design)  

COURSE STRUCTURE  
(R18 Regulations applicable for the batches admitted from Academic Year 2018-19 onwards)  

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VAAGDEVI COLLEGE OF ENGINEERING
(AUTONOMOUS)

(M18VL01) CMOS DIGITAL INTEGRATED CIRCUIT DESIGN

M. Tech: I- Semester

UNIT –I:
MOS Design
Pseudo NMOS Logic – Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

UNIT –II:
Combinational MOS Logic Circuits:
MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, Complex Logic circuits design – Realizing Boolean expressions using NMOS gates and CMOS gates, AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

UNIT –III:
Sequential MOS Logic Circuits:
Behavior of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flipflop.

UNIT –IV:
Dynamic Logic Circuits:
Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

UNIT –V:
Semiconductor Memories:
Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory- NOR flash and NAND flash.

TEXT BOOKS:

REFERENCE BOOKS:

COURSE OUTCOMES:
After the completion of this course, the students should be able to
- Define the basic of CMOS technology
- Relate, compare, interpret and make the use of the best CMOS design techniques for

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implementation, analysis & design of Combinational MOS logic circuits

- Know & tell different types of memories and compare performance evaluation of each memory modules so they can be able to think & justify how to improve performance by taking different structures.
- Define, simplify & justify which dynamic logic circuit can be used investigate CMOS circuits.
- Recommend various CMOS techniques and also other device technologies based on circuit constraints requirement.

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COURSE OBJECTIVES:
- To understand the fundamentals of IC technology.
- To understand the analysis and design of analog integrated circuits starting from basic building blocks to different implementations of the amplifiers in CMOS technology.

UNIT –I:
MOS Devices and Modeling

UNIT –II:
Analog CMOS Sub-Circuits:
MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

UNIT –III:
CMOS Amplifiers:
Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain, Amplifiers Architectures.

UNIT –IV:
CMOS Operational Amplifiers:

UNIT –V:
Comparators:
Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop-Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

TEXT BOOKS:

REFERENCE BOOKS:
2. CMOS: Circuit Design, Layout and Simulation- Baker, Li and Boyce, PHI.

COURSE OUTCOMES:
Upon completion of this course, students should demonstrate the ability to:
• Define the parameters of MOS Devices & can predict the performance or behavior of Analog VLSI circuit.
• Use mathematical models of MOS transistors to evaluate their behavior in analog circuits & selects suitable design approaches while trading off conflicting requirements
• Analyze & characterize analog devices and systems & Designing CMOS analog circuits to achieve performance specifications
• Understand design issues related to analog VLSI system &working of MOS based data converter circuits.
• Make the significant use of knowledge of subject in research or on project in VLSI domain.

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M.Tech-VLSI System Design

VAAGDEVI COLLEGE OF ENGINEERING
(AUTONOMOUS)
(M18VL03) DIGITAL SYSTEM DESIGN USING HDL
(Program Elective – I)

M. Tech: I-Semester

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COURSE OBJECTIVES:
- To understand the different abstract levels in Verilog for modeling digital circuits.
- The student will learn the basic CMOS circuit, characteristics and performance.
- The student will learn the designing of combinational and sequential circuits in CMOS.

UNIT I - BASIC CONCEPTS - VERILOG
Operators, Basic concepts, Identifiers, System task and functions, Value set, Data types, Parameters, Operands, Operators, Modules and ports, Gate-level Modeling, Dataflow Modeling, Behavioral Modeling, Switch level modeling, Tri state gates, MOS Switches, Bidirectional switches, User defined primitives, Combinational UDP, Sequential UDP. Introduction to synthesis, Verilog HDL synthesis-Synthesis Design flow Test bench-lab exercise.

UNIT II – BASICS OF MOS TRANSISTORS
MOS transistors- Threshold voltage- characteristics of MOS transistor-channel length modulation- short channel effects- Design of Logic gates using NMOS, PMOS and CMOS, Stick diagrams- Transfer characteristics of CMOS inverter- Power dissipation – Delay and sizing of inverters- Lab exercise.

UNIT III - CMOS – COMBINATIONAL CIRCUITS
Static CMOS design-complementary CMOS - static properties-complementary CMOS design-Power consumption in CMOS logic gatingdesign or glitching transitions - Design techniques to reduce switching activity - Radioed logic-DC VSL - pass transistor logic - Differential pass transistor logic -Sizing of level restorer-Sizing in pass transistor-Dynamic CMOS design-Basic principles - Domino logic-optimization of Domino logic-NPCMOS-logic style selection - Designing logic for reduced supply voltages. Lab exercise in Switch level modeling.

UNIT IV - CMOS – SEQUENTIAL CIRCUITS
Timing metrics for sequential circuit - latches Vs registers -static latches and registers - Bistability principle - multiplexer based latches-master slave edge triggered registers- non-ideal clock signals-low voltage static latches-static SR flip flop - Dynamic latches and registers-C2MOS register - Dual edge registers-True single phase clocked registers-pipelining to optimize sequential circuit latch Vs register based pipelines-non-Bistable sequential circuit-Schmitt trigger-mono stable -Astable -sequential circuit - choosing a clocking strategy.. Lab exercise in Switch level modeling

UNIT V – SUB-SYSTEM DESIGN/ SYSTEM VERILOG

REFERENCES

Department of ECE
COURSE OUTCOMES:
Upon completion of this course, students should demonstrate the ability to:

- Design and analyze combinational, sequential and arithmetic circuits using HDL.
- Understand digital system design flow, timing, synthesis and FPGA implementation issues.
- Solve engineering problems in the area of digital system design & Examine or Inspect for an optimum layout for IC layout at VLSI backend design.
- Design, analyze & can predict the performance characteristics of logic gates using NMOS, PMOS & CMOS technology at VLSI backend design.
- Tell an optimum trade with respect to three basic parameters of VLSI design for VLSI circuit at frontend or backend VLSI design

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M.Tech-VLSI System Design

VAAGDEVI COLLEGE OF ENGINEERING
(AUTONOMOUS)

(M18VL04)VLSI SIGNAL PROCESSING
(Program Effective – I)

M. Tech: I-Semester

COURSE OBJECTIVES:
• To understand the fundamentals of DSP
• To learn various DSP structures and their implementation.
• To know designing constraints of various filters.

UNIT I - INTRODUCTION TO DIGITAL SIGNAL PROCESSING:
Linear System Theory- Convolution- Correlation - DFT- FFT- Basic concepts in FIR Filters and IIR Filters- Filter Realizations. Representation of DSP Algorithms-Block diagram-SFG-DFG.

UNIT II - ITERATION BOUND, PIPELINING AND PARALLEL PROCESSING OF FIR FILTER:

UNIT III - FAST CONVOLUTION AND ARITHMETIC STRENGTH REDUCTION IN FILTERS:

UNIT IV - PIPELINED AND PARALLEL RECURSIVE FILTERS:
Pipeline Interleaving in Digital Filters- Pipelining in 1st Order IIR Digital Filters- Pipelining in Higher- Order IIR Filters-Clustered Look ahead and Stable Clustered Look ahead- Parallel Processing for IIR Filters and Problems.


REFERENCES

COURSE OUTCOMES:
Upon completion of this course, students should demonstrate the ability to:

• Apply the concepts of pipelining, parallel processing, retiming, folding and unfolding to optimize digital signal processing architectures
• Use of proper techniques for parallel processing design for scaling and round off noise

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• Apply all techniques to improve implementations of several DSP algorithms, using both ASICs and off-the-shelf programmable digital signal processors
• Design high-speed, low-area, and low-power VLSI systems for a broad range of DSP applications
• Minimize the computational complexity using fast convolution algorithms & Make the significant use of knowledge of subject in research or on project in VLSI domain

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M.Tech-VLSI System Design

VAAGDEVI COLLEGE OF ENGINEERING
(AUTONOMOUS)

(M18VL05) VLSI TECHNOLOGY
(Program Elective – I)

M. Tech: I-Semester

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COURSE OBJECTIVES:

- To understand the impact of the physical and chemical processes of integrated circuit fabrication technology on the design of integrated circuits.
- To understand physics of the Crystal growth, wafer fabrication and basic properties of silicon wafers.
- To Learn the concepts of Design rules and Scaling, BICMOS ICs.

UNIT – I:
Review of Microelectronics and Introduction to MOS Technologies:
MOS, CMOS, BiCMOS Technology. Basic Electrical Properties of MOS, CMOS & BiCMOS Circuits: Ids – Vds relationships, Threshold Voltage VT, Gm, Gds and ωo, Pass Transistor, MOS, CMOS & Bi CMOS Inverters, Zpu/Zpd, MOS Transistor circuit model, Latch-up in CMOS circuits.

UNIT – II:
Layout Design and Tools:

UNIT – III:
Overview of semiconductor industry, Stages of Manufacturing, Process and product trends, Crystal growth, Basic wafer fabrication operations, process yields, Semiconductor material preparation, Basic wafer fabrication operations, Yield measurement, Contamination sources, Clean room construction, Oxidation and Photolithography, Doping and Depositions, Metallization. Ten step patterning process, Photoresists, physical properties of photoresists, Storage and control of photoresists, photo masking process, Hard bake, develop inspect, Dry etching Wet etching, resist stripping

UNIT – IV
Doping and depositions: Diffusion process steps, deposition, Drive-in oxidation, Ion implantation-1, Ion implantation-2, CVD basics, CVD process steps, Low pressure CVD systems, Plasma enhanced CVD systems, Vapour phase epitoxy, molecular beam epitaxy.

UNIT – V
Design rules and Scaling, BICMOS ICs: Choice of transistor types, pnp transistors, Resistors, capacitors, Packaging: Chip characteristics, package functions, package operations

TEXT BOOKS:

REFERENCE BOOKS:
2. Eugene D. Fabricius, Introduction to VLSI design, McGraw Hill, 1999

COURSE OUTCOMES:
Upon completion of this course, students should demonstrate the ability to:

- Build circuits using IC’s.
- In depth knowledge of applying the concepts in real time applications.
- Understand the main elements of hierarchical IC design namely interested circuit technology, approaches to system design, architectural issues.
- Design implementation and layout & Use of tools for efficient designing.
- Make the significant use of knowledge of subject in research or on project in VLSI domain.

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COURSE OBJECTIVES:
- Understand the concepts of Physical Design Process such as partitioning, Floorplanning, Placement and Routing.
- Discuss the concepts of design optimization algorithms and their application to physical design automation.
- Understand the concepts of simulation and synthesis in VLSI Design Automation.
- Formulate CAD design problems using algorithmic methods.

UNIT I:
PRELIMINARIES
Introduction to Design Methodologies, Design Automation tools, Algorithmic Graph Theory, Computational complexity, Tractable and Intractable problems.

UNIT II:
GENERAL PURPOSE METHODS FOR COMBINATIONAL OPTIMIZATION
Backtracking, Branch and Bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu search, Genetic Algorithms.

UNIT III:
LAYOUT COMPACTION, PLACEMENT, FLOORPLANNING AND ROUTING
Problems, Concepts and Algorithms.
MODELLING AND SIMULATION
Gate Level Modelling and Simulation, Switch level Modelling and Simulation.

UNIT IV:
LOGIC SYNTHESIS AND VERIFICATION
Basic issues and Terminology, Binary-Decision diagrams, Two-Level logic Synthesis
HIGH-LEVEL SYNTHESIS

UNIT V:
PHYSICAL DESIGN AUTOMATION OF FPGAs
FPGA technologies, Physical Design cycle for FPGAs, partitioning and Routing for segmented and staggered Models.

PHYSICAL DESIGN AUTOMATION OF MCMs
TEXT BOOKS

REFERENCE BOOKS

COURSE OUTCOMES:
Upon completion of this course, students should demonstrate the ability to:

- Describe and formulate the flow of VLSI Design for any application.
- Explain the algorithms for partitioning, floor planning, placement and routing the digital designs at frontend level & at backend VLSI Design level.
- Compare the various scheduling algorithms & Analyze & solve the issues related to logic synthesis & verification
- Explain the algorithms for partitioning, floor planning, placement and routing the MCM modules
- Make significant contribution in the research in based on design of CAD tool for VLSI design

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COURSE OBJECTIVES:
- To introduce students to the modern embedded systems and to show how to understand and program such systems using a concrete platform built around a modern embedded processor like the Intel ATOM.
- To introduce the students to Embedded Firmware.
- To understand the concepts of RTOS based Embedded design.

UNIT –I:
Introduction to Embedded Systems

UNIT –II:
Typical Embedded System:
Core of the Embedded System: General Purpose and Domain Specific Processors, ASICs, PLDs, Commercial Off-The-Shelf Components (COTS), Memory: ROM, RAM, Memory according to the type of Interface, Memory Shadowing, Memory selection for Embedded Systems, Sensors and Actuators, Communication Interface: Onboard and External Communication Interfaces.

UNIT –III:
Embedded Firmware:
Reset Circuit, Brown-out Protection Circuit, Oscillator Unit, Real Time Clock, Watchdog Timer, Embedded Firmware Design Approaches and Development Languages.

UNIT –IV:
RTOS Based Embedded System Design:
Operating System Basics, Types of Operating Systems, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling.

UNIT –V:
Task Communication: Shared Memory, Message Passing, Remote Procedure Call and Sockets, Task Synchronization: Task Communication/Synchronization Issues, Task Synchronization Techniques, Device Drivers, How to Choose an RTOS.

TEXT BOOKS:

REFERENCE BOOKS:
1. Embedded Systems – Raj Kamal, TMH.

COURSE OUTCOMES:
Upon completion of this course, students should demonstrate the ability to:
Know the Basic Concept of Embedded Systems.
Interpret the difference between Microcontrollers and Microprocessors.
Apply the Software for Embedded System Design & concepts of Embedded OS.
Explain and apply the concept of Embedded Firmware, RTOS Based Embedded System Design and Task function.
Make significant contribution in the research in applications based on embedded system design.

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VAAGDEVI COLLEGE OF ENGINEERING
(AUTONOMOUS)

(M18VL08) DEVICE MODELLING
(Program Elective – II)

M. Tech: I-Semester

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COURSE OBJECTIVES:
- To make the student understand how MOSFET and other semiconductor devices are modeled
- To impart knowledge to simulate MOSFET for various operational requirements.
- To impart a knowledge on advanced structures of MOSFETs like SOIFET, FinFET etc.

UNIT - I:
Introduction to Semiconductor Physics:
Review of Quantum Mechanics, Boltzman transport equation, Continuity equation, Poisson equation.

Integrated Passive Devices:
Types and Structures of resistors and capacitors in monolithic technology, Dependence of model parameters on structures

UNIT - II: Integrated Diodes:
Junction and Schottky diodes in monolithic technologies – Static and Dynamic behavior – Small and large signal models – SPICE models

Integrated Bipolar Transistor:
Types and structures in monolithic technologies – Basic model (Eber-Moll) – Gunmel - Poon model-dynamic model, Parasitic effects – SPICE model – Parameter extraction

UNIT - III:
Integrated MOS Transistor:
NMOS and PMOS transistor – Threshold voltage – Threshold voltage equations – MOS device equations – Basic DC equations second order effects – MOS models – small signal AC characteristics – MOS FET SPICE model level 1, 2, 3 and 4

UNIT - IV:

UNIT - V:
Modeling of Hetero Junction Devices: Band gap Engineering, Band gap Offset at abrupt Hetero Junction, Modified current continuity equations, Hetero Junction bipolar transistors (HBTs), SiGe

TEXT BOOKS:

REFERENCE BOOKS:
2. Introduction to Device Modeling and Circuit Simulation – Tor A. Fijedly, Wiley-

COURSE OUTCOMES:
Upon completion of this course, students should demonstrate the ability to:

- Understand the physics of and design elements of silicon MOSFETs.
- Explain the equations, approximations and techniques available for deriving a model with specified properties, for a general device characteristic with known qualitative theory.
- Analyze the performance issues & inherent trade off involved in system design Offer clues to qualitative understanding of the physics of a new device and conversion of this understanding into equations.
- Utilize semiconductor models to analyze carrier densities and carrier transport & Simulate characteristics of a simple device using MATLAB, SPICE and SYNOPSYS.
- Understand and analyze the inner working of semiconductor p-n diodes, Schottky barrier diodes and advanced MOSFET technology.

***
M. Tech: I-Semester

Course Objectives:
- To understand the nuances of language and vocabulary in writing a Research Paper.
- To develop the content, structure and format of writing a research paper.
- To give the practice of writing a Research Paper.
- To enable the students to evolve original research papers without subjected to plagiarism.

UNIT I:

UNIT II:
RESEARCH FORMAT: Title – Abstract – Introduction – Discussion - Findings – Conclusion – Style of Indentation – Font size/Font types – Indexing – Citation of sources.

UNIT III:

UNIT IV:

UNIT V:
HOW TO & WHERE TO GET PUBLISHED: Reputed Journals – National/International – ISSN No, No. of volumes, Scopes Index/UGC Journals – Free publications - Paid Journal publications – /Advantages/Benefits

TEXT BOOKS:

REFERENCES:
1. NPTEL: https://onlinecourses.nptel.ac.in/noc18_mg13/preview

COURSE OUTCOMES:
- Upon completion of this course, students should demonstrate the ability to:
• Understand the nuances of language and vocabulary in writing a Research Paper
• Develop the content, structure and format of writing a research paper
• Analyze and practice writing a Research Paper
• Enable the students to plan for original research papers without subjected to plagiarism.

****
M. Tech: I-Semester

Course Objectives:
- To develop an understanding of IPR/ research methodology in the process of creation of patents through research.
- To develop further research capabilities.
- To learn better report writing skills and Patenting.

UNIT I:
RESEARCH METHODOLOGY: Objectives and Motivation of Research, Significance of Literature review, Types of Research, Research Approaches, and Research Methods verses Methodology, Research and Scientific Method, Importance of Research Methodology, Research Process, Criteria of Good Research.

UNIT II:

UNIT III:

UNIT IV:

UNIT V:

TEXT BOOKS:

REFERENCES:

Department of ECE
-22-
COURSE OUTCOMES:

- Upon completion of this course, students should demonstrate the ability:
- Develop an understanding of IPR/ research methodology in the process of creation of patents through research
- Develop further research capabilities
- Design Important Concepts Related to Research Design
- Learn better report writing skills and Patenting.

***

Department of ECE
-23-
VAAGDEVI COLLEGE OF ENGINEERING  
(AUTONOMOUS) 

(M18VL09) HDL PROGRAMMING LABORATORY 

M. Tech: I-Semester  

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Note: Any 10 of the following digital/analog circuits are to be designed and implemented using Xilinx/Altera/Equivalent CAD tools.

Programming can be done using any complier. Down load the programs on FPGA/CPLD boards and performance testing may be done apart from verification by simulation with any of the front end tools.

**COURSE OBJECTIVES:**
- To design Various Combinational and Sequential circuits using VHDL
- To design Various Combinational and Sequential circuits using Verilog HDL.
- To verify different logic circuits using FPGA/CPLD Boards.

**List of Experiments:**
1. Design and Simulate Combinational circuits in all three modeling of VHDL
2. Design and Simulate 4-bit adder in structural and behavioral modeling VHDL
3. Design and Simulate sequential circuits using VHDL.
4. Design and Simulate State machine using VHDL.
5. Design and Simulate Traffic Light Controller using VHDL.
7. Design and Simulate ALU using Packages and user defined data type.
8. Design and Simulate Flip-flops using VHDL
9. Design and Simulate Combinational circuits using Verilog HDL
10. Design and Simulate Sequential circuits using Verilog HDL
11. Design and Simulate logic gates using Switch level modeling
12. FPGA implementation of combinational circuit using VHDL and Verilog HDL

**COURSE OUTCOMES:**
Upon completion of this course, students should demonstrate the ability:

- Apply the knowledge in Simulation and Synthesis of Digital Circuits.
- Design Various Combinational and Sequential circuits using Verilog HDL & HDL
- Explain the System Modeling with Tasks and Functions.
- Design of digital circuits using FPGA/CPLD boards.

***
M.Tech-VLSI System Design

VAAGDEVI COLLEGE OF ENGINEERING
(AUTONOMOUS)

(M18VL10) DIGITAL IC DESIGN LABORATORY

M. Tech: I-Semester

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Note: Any 10 of the following digital/analog circuits are to be designed and implemented using Mentor Graphics / Tanner Tools/Microwind-DSCH/Equivalent CAD tools.

COURSE OBJECTIVES:
- To design Various Combinational circuits using CMOS Logic.
- To design Various Sequential circuits using CMOS Logic.
- To design Various circuits using Different Logic Styles.
- To design Layout of Different logic circuits.

List of Experiments:
1. Design and Simulation of CMOS/NMOS Inverter.
2. Design and Simulation of CMOS Universal Gates.
3. Design and Simulation of Full Adder and Full Subtractor.
4. Design and Simulation of Domino Logic and NORA Logic.
5. Design and Simulation of Dynamic Logic and Pseudo NMOS Logic.
6. Design and Simulation of Transmission Gate and Pass Transistor Logic.
7. Design and Simulation of Bi-CMOS Inverter.
8. Design and Simulation of Bi-CMOS NAND/NOR Logic.
9. Design and Simulation of SRAM Design.
10. Design and Simulation DRAM Design.
11. Post Layout Simulation CMOS Inverter.

COURSE OUTCOMES:
- Design CMOS inverters, logic circuits and transmission gates to specifications.
- Design latches and flip-flops as the basic circuit for Random-Access Memory (RAM) and Read-Only-Memory (ROM) cells.
- Understand the Design of Bi-CMOS Inverter, logic circuits.
- Design post Layout of Different logic circuits.

***
VAAGDEVI COLLEGE OF ENGINEERING
(AUTONOMOUS)

(M18VL11) CMOS MIXED SIGNAL CIRCUIT DESIGN

M. Tech:II-Semester

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COURSE OBJECTIVES:
• To know mixed signal circuits like DAC, ADC, PLL etc.
• To gain knowledge on filter design in mixed signal mode.
• To acquire knowledge on design different architectures in mixed signal mode.

UNIT -I:
Switched Capacitor Circuits:
Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing, biquad filters.

UNIT -II:
Phased Lock Loop (PLL):
Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs-PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications.

UNIT -III:
Data Converter Fundamentals:
DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters.

UNIT -IV:
Nyquist Rate A/D Converters:

UNIT -V:
Oversampling Converters:
Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multibit quantizers, Delta sigma D/A

TEXT BOOKS:

REFERENCE BOOKS:
COURSE OUTCOMES:
After completing this course the students should be able to:

- Build mixed signal circuits like DAC, ADC, PLL etc & Gain knowledge on filter design in mixed signal mode & To acquire knowledge on design different architectures in mixed signal mode.
- Analyze digital test and linear test engineers to the mixed signal world by teaching the basics of analog and mixed signal test methods. Sampling Theory, Frequency Domain Testing, and Digital Signal Processing
- Apply these fundamental concepts to different test methods and data validation for mixed signal parameters together with debugging, noise reduction and device interface techniques.
- Deal with the theory and design skills of CMOS op-amps, voltage reference circuits, switched capacitor circuits, sample-and- hold circuits, and A/D & D/A converters used in modern communication systems and consumer electronic products.
- Design of core mixed-signal IC blocks: comparators and data converters & System level design flow: top-down and bottom-up design methodologies

***
VAAGDEVI COLLEGE OF ENGINEERING
(AUTONOMOUS)

(M18VL12)VLSI DESIGN VERIFICATION AND TESTING

M. Tech:II-Semester

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COURSE OBJECTIVES:
- To gain knowledge on digital testing as applied to VLSI design.
- To acquire knowledge on testing of algorithms for digital circuits.
- To learn various testing methods for digital circuits.

UNIT -I:
Introduction to Testing:

UNIT -II:
Logic and Fault Simulation:

UNIT -III:
Testability Measures:
SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

UNIT -IV:
Built-In Self-Test:
The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per-Scan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST.

UNIT -V:
Boundary Scan Standard:
Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

TEXT BOOKS:

REFERENCE BOOKS:

COURSE OUTCOMES:
After completing this course the students should be able to:
- Gain knowledge on digital testing as applied to VLSI design &Acquire knowledge on
testing of algorithms for digital circuits.

- Learn various testing methods for digital circuits & process of modern VLSI design, verification, and test.
- Develop and understanding for the advanced design concepts in modern VLSI technologies & Learn self-checking circuits where faults are detected by subcircuit called checker.
- Gain the knowledge of testing and verification in VLSI design process, ATPG concepts for combinational and sequential circuits.
- Specific techniques for designing high-speed, low-power, and easily-testable circuits.
M.Tech-VLSI System Design

(Course Elective – III)

M. Tech:II-Semester

COURSE OBJECTIVES:
- To design Low power CMOS designs, for digital circuits.
- To gain knowledge on low power circuit design styles for VLSI circuits.
- To understand power estimation and optimization methods for VLSI circuits.

UNIT –I:
Fundamentals:

UNIT –II:
Low-Power Design Approaches:
Switched Capacitance Minimization Approaches:
System Level Measures, Circuit Level Measures, Mask level Measures.

UNIT –III:
Low-Voltage Low-Power Adders:

UNIT –IV:
Low-Voltage Low-Power Multipliers:
Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh- Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

UNIT –V:
Low-Voltage Low-Power Memories:

TEXT BOOKS:
2. Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering.

COURSE OUTCOMES:
After completing this course the students should be able to:

- Design Low power CMOS designs, for digital circuits & Gains knowledge on low power circuit design styles for VLSI circuits.
- Understand power estimation and optimization methods for VLSI circuits & causes of the power dissipation in digital ICs.
- Exploring the low power circuits and architectures for VLSI system.
- Understand the concept of VLSI circuit of low power operation & case study of low power design
- Design various circuits for optimize power
COURSE OBJECTIVES:

- To gain knowledge on Optimization techniques involved in VLSI circuits.
- To explore various Statistical modeling and performance analysis of VLSI Circuits.
- To understand the Concept of Genetic Algorithms and Routing Procedures.

UNIT – I:
Statistical Modeling:
Modeling sources of variations, Monte Carlo techniques, Process variation modeling- Pelgrom’s model, Principle component based modeling, Quad tree based modeling, Performance modeling-Response surface methodology, delay modeling, interconnect delay models.

UNIT – II:
Statistical Performance, Power and Yield Analysis
Statistical timing analysis, parameter space techniques, Bayesian networks Leakage models, High level statistical analysis, Gate level statistical analysis, dynamic power, leakage power, temperature and power supply variations, High level yield estimation and gate level yield estimation.

UNIT – III:
Convex Optimization:
Convex sets, convex functions, geometric programming, trade-off and sensitivity analysis, Generalized geometric programming, geometric programming applied to digital circuit gate sizing, Floor planning, wire sizing, Approximation and fitting- Monomial fitting, Maxmonomial fitting, Posynomial fitting.

UNIT – IV:
Genetic Algorithm:

UNIT – V:
GA Routing Procedures and Power Estimation:

TEXT BOOKS / REFERENCE BOOKS:
COURSE OUTCOMES:
After completing this course the students should be able to:
• Gain knowledge on Optimization techniques involved in VLSI circuits.
• Analyze methods of optimization to engineering students, including linear programming, nonlinear programming, and heuristic methods
• Understand balance between theory, numerical computation, problem setup for solution by optimization software, and applications to engineering systems.
• Studies General optimization algorithm; necessary and sufficient conditions for optimality
• Demonstrate the Concept of Genetic Algorithms and Routing Procedures

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VAAGDEVI COLLEGE OF ENGINEERING  
(AUTONOMOUS)  

(M18VL15) HIGH SPEED VLSI DESIGN  
(Program Elective – III)  

M. Tech:II-Semester  

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COURSE OBJECTIVES:  
- To gain knowledge on circuits and techniques involved in high speed VLSI circuits.  
- To explore various design strategies to be followed for designing a high speed VLSI circuits.  
- To understand the logic styles for designing a high speed VLSI circuit.  

UNIT I - CLOCKED LOGIC STYLES:  
Clocked Logic Styles, Single-Rail Domino Logic Styles, Dual-Rail Domino Structures, Latched Domino Structures, Clock pass Gate Logic Non Clocked Logic Styles, Static CMOS, DCVS Logic, Non-Clocked pass Gate Families.  

UNIT II - CIRCUIT DESIGN MARGINING AND DESIGN VARIABILITY:  
Circuit Design Margining, Design Induced Variations, Process Induced Variations, Application Induced Variations, Noise.  

UNIT III - LATCHING STRATEGIES:  

UNIT IV - INTERFACE TECHNIQUES:  
Signaling Standards, Chip-to-Chip Communication Networks, ESD Protection, Skew Tolerant Design  

UNIT V - CLOCKING STYLES:  
Clocking Styles, Clock Jitter, Clock Skew, Clock Generation, Clock Distribution, Asynchronous Clocking Techniques.  

REFERENCES  
2. Evan Sutherland, Bob Stroll, David Harris,” Logical Efforts, Designing Fast CMOS Circuits”, Kluwer Academic Publishers, 1999  

COURSE OUTCOMES:  
After completing this course the students should be able to:  
- Gain knowledge on circuits and techniques involved in high speed VLSI circuits.  
- Explore various design strategies to be followed for designing a high speed VLSI circuits.  
- Understand the logic styles for designing a high speed VLSI circuit & Learn the basics of VLSI design for high speed processing  
- Apply methods for logical efforts, logic styles, latching strategies, interface techniques and related issues.  
- Acquire knowledge about High Speed VLSI Circuits Design & Learn the basics of VLSI design for high speed processing  

**
VAAGDEVI COLLEGE OF ENGINEERING
(AUTONOMOUS)

(M18VL16)ASIC DESIGN
(Program Elective – IV)

M. Tech:II-Semester

COURSE OBJECTIVES:
- To learn the fundamentals of ASIC and its design methods
- To gain knowledge on programmable architectures for ASICs
- To understand the physical design of ASIC.

UNIT I - INTRODUCTION TO ASIC’S
Types of ASICs - Design flow - CMOS transistors CMOS Design rules - Combinational Logic Cell - Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort - Library cell design - Library architecture.

UNIT II - PROGRAMMABLE ASIC’S
Anti fuse - static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT - Xilinx LCA -Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs – Xilinx I/O blocks.

UNIT III - PROGRAMMABLE ASIC LOGIC CELLS

UNIT IV - ASIC FLOOR PLANNING, PLACEMENT AND ROUTING

UNIT V - OPTIMIZATION ALGORITHMS
Planar subset problem(PSP) -single layer global routing single layer detailed routing wire length and bend minimization technique -over the cell(OTC) Routing-multichip modules(MCM)- Programmable logic arrays-Transistor chaining-Weinberger Arrays-Gate Matrix Layout-1D compaction-2D compaction

REFERENCES

COURSE OUTCOMES:
After completing this course the students should be able to
- To learn the fundamentals of ASIC and its design methods
- To gain knowledge on programmable architectures for ASICs & physical design of ASIC
- To prepare the student to be an entry level industrial standard cell ASIC or FPGA designer
- To give the student an understanding of issues and tools related to ASIC/FPGA design.
• Prepare the student for implementation, including timing, performance and power optimization, verification and manufacturing test

***
COURSE OBJECTIVES:
- To learn System on chip fundamentals, their applications.
- To gain knowledge on SOC design.
- To learn the various computation models of SOCs.

UNIT –I:
Introduction to the System Approach:

UNIT –II:
Processors:

UNIT –III:
Memory Design for SOC:

UNIT –IV:
Interconnect Customization and Configuration:

UNIT –V:
Application Studies / Case Studies:
SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.

TEXT BOOKS:

Department of ECE
REFERENCE BOOKS:
2. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM.

COURSE OUTCOMES:
After completing this course the students should be able to:
- To learn the fundamentals of ASIC and its design methods
- To gain knowledge on programmable architectures for ASICs & physical design of ASIC
- To prepare the student to be an entry level industrial standard cell ASIC or FPGA designer
- To give the student an understanding of issues and tools related to ASIC/FPGA design.
- Prepare the student for implementation, including timing, performance and power optimization, verification and manufacturing test

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VAAGDEVI COLLEGE OF ENGINEERING  
(AUTONOMOUS) 
(M18VL18)SEMICONDUCTOR MEMORY DESIGN AND TESTING  
(Program Elective – IV) 

M. Tech:II-Semester  

COURSE OBJECTIVES:  
- To know the design of MOS memories and the various precautionary methods to be used in their design.  
- To gain knowledge on various testing methods of semiconductor memories.  
- To get an overview on reliability of semiconductors and their testing. 

UNIT -I: 
Random Access Memory Technologies: 
SRAM – SRAM Cell structures, MOS SRAM Architecture, MOS SRAM cell and peripheral circuit operation, Bipolar SRAM technologies, SOI technology, Advanced SRAM architectures and technologies, Application specific SRAMs, DRAM – DRAM technology development, CMOS DRAM, DRAM cell theory and advanced cell structures, BICMOS DRAM, soft error failure in DRAM, Advanced DRAM design and architecture, Application specific DRAM 

UNIT -II: 
Non-volatile Memories: 
Masked ROMs, High density ROM, PROM, Bipolar ROM, CMOS PROMS, EPROM, Floating gate EPROM cell, One time programmable EPROM, EEPROM, EEPROM technology and architecture, Non-volatile SRAM, Flash Memories (EPROM or EEPROM), advanced Flash memory architecture 

UNIT -III: 
Memory Fault Modeling Testing and Memory Design for Testability and Fault Tolerance: 
RAM fault modeling, Electrical testing, Pseudo Random testing, Megabit DRAM Testing, non-volatile memory modeling and testing, IDDQ fault modeling and testing, Application specific memory testing, RAM fault modeling, BIST techniques for memory 

UNIT -IV: 
Semiconductor Memory Reliability and Radiation Effects: 
General reliability issues RAM failure modes and mechanism, Non-volatile memory reliability, reliability modeling and failure rate prediction, Design for Reliability, Reliability Test Structures, Reliability Screening and qualification, Radiation effects, Single Event Phenomenon (SEP), Radiation Hardening techniques, Radiation Hardening Process and Design Issues, Radiation Hardened Memory characteristics, Radiation Hardness Assurance and Testing, Radiation Dosimetry, Water Level Radiation Testing and Test structures 

UNIT -V: 
Advanced Memory Technologies and High-density Memory Packing Technologies: 
Ferroelectric RAMs (FRAMs), GaAs FRAMs, Analog memories, magneto resistive RAMs (MRAMs), Experimental memory devices, Memory Hybrids and MCMs (2D), Memory Stacks and MCMs (3D), Memory MCM testing and reliability issues, Memory cards, High Density Memory Packaging Future Directions 

TEXT BOOKS:  

COURSE OUTCOMES:
After completing this course the students should be able to:

- Know the design of MOS memories and the various precautionary methods to be used in their design
- Learn overview of memory chip design, DRAM circuits, voltage generators, performance analysis and design issues of ultra-low voltage memory circuits
- Acquire knowledge about High-Performance Subsystem Memories & Analyse RAM and DRAM Design
- Demonstrate Advanced Memory Technologies and High-density Memory Packing Technologies & Gains knowledge on various testing methods of semiconductor memories
- Get an overview on reliability of semiconductors and their testing

***
M.Tech: II-Semester

Course Objectives:
- This course provides understanding stress such as work related stress and individual stress
- This course serves time management such as importance of planning the day and developing concentration
- This course serves career plateau such as Identifying Career plateaus and Structural and Content Plateauing and Making a fresh start
- This course provides controlling crisis management
- This course provides self development

UNDERSTANDING STRESS

TIME MANAGEMENT
Techniques – Importance of Planning the day –developing concentration – Prioritizing Beginning at the start – Techniques for conquering procrastination – Sensible delegation – Taking the right breaks – Learning to say “No”

CAREER PLATEAU

CRISIS MANAGEMENT

SELF DEVELOPMENT
Improving personality – Leading with Integrity – Enhancing Creativity – Effective decision making – Sensible Communication – The Listening Game – Managing Self – Mediation for peace – Yoga for Life

TEXT BOOKS

REFERENCES
1. Jeffr Davison, Managing Stress, Prentice Hall of India, New Delhi
COURSE OUTCOMES:

• Enhance of Physical strength and flexibility.
• Learn to relax and focus.
• Relieve physical and mental tension
• Improve work performance/ efficiency.

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Note: Any 10 of the following digital/analog circuits are to be designed and implemented using Mentor Graphics / Tanner Tools/Microwind-DSCH/NG-Spice/Equivalent CAD tools.

COURSE OBJECTIVES:
- To design Various Characteristics of MOS Logic.
- To design Various Amplifier circuits using CMOS Logic.
- To design Various circuits using Different Logic Styles.
- To design Layout of Different logic circuits.

List of Experiments:
1. Design of DC Characteristics of MOS Transistor.
2. Design and simulation of MOS current sources and current mirrors.
3. Design and simulation of emitter follower circuit.
5. Design and simulation of Clippers and Clampers
7. Design and simulation of any circuit using current sink load.

COURSE OUTCOMES:
After completing this course the students should be able to:

- Design Various Characteristics of MOS Logic
- Design Various Amplifier circuits using CMOS Logic
- Design Various circuits using Different Logic Styles
- Design Layout of Different logic circuits

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VAAGDEVI COLLEGE OF ENGINEERING
(AUTONOMOUS)

(M18VL20) MIXED SIGNAL VLSI LABORATORY

M. Tech: II-Semester

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Note: Any 10 of the following digital/analog circuits are to be designed and implemented using Mentor Graphics / Tanner Tools/Microwind-DSCH/NG-Spice/Equivalent CAD tools.

COURSE OBJECTIVES:

- To design Various Amplifier circuits using CMOS Logic.
- To design Various Complex circuits using Different Logic Styles.
- To design Layout of Different logic circuits.

List of Experiments:

1. SPICE simulation of Cascode Amplifier.
2. SPICE simulation of Differential Amplifier using Switched capacitor.
3. SPICE simulation of Two stage Operational Amplifier.
4. SPICE simulation of Two stage Comparator Circuit
5. SPICE simulation of Inverting Amplifier.
6. SPICE simulation Sample and Hold Circuit.
7. SPICE simulation of PLL.
8. SPICE simulation of Latches/Flip flops using CMOS.
9. SPICE simulation of Combinational Circuit using Bi-CMOS Logic.
10. Post Layout Simulation of Combinational Circuit
11. Post Layout Simulation of Sequential Circuit.

COURSE OUTCOMES:

After completing this course the students should be able to:

- Design Various Amplifier circuits using CMOS Logic
- Design Various Complex circuits using Different Logic Styles
- Design Layout of Different logic circuits
- Digital/analog circuits are to be designed and implemented using CAD tools.

***
COURSE OUTCOMES:

After the completion of this course, the students should be able to:

- Use fundamental knowledge and skills in engineering and apply it effectively on a project.
- Understand the Product Development Process including budgeting through Mini Project.
- Plan for various activities of the mini project.
- Inculcate electronic hardware and software implementation skills.
- Manage any disputes and conflicts within and outside individually.
- Prepare a technical report based on the Mini project.
- Deliver technical seminar based on the Mini Project work carried out.
COURSE OBJECTIVES:

- To know the various methods for implementation of DSP systems.
- To understand the various implementations of VLSI DSP architectures for Arithmetic operations
- To gain knowledge on low power DSP architectures.

UNIT I – UNFOLDING:


UNIT II - DIGITAL MULTIPLIER ARCHITECTURES:

Parallel Multipliers- Interleaved Floor-plan and Bit-Plane-Based Digital Filters- Bit-Serial Multipliers- Bit-serial Filter Design and ImplementationCanonic Signed Digit Arithmetic- Distributed Arithmetic.

UNIT III - REDUNDANT ARITHMETIC:


UNIT IV - SYNCHRONOUS AND ASYNCHRONOUS PIPELINING:

Synchronous Pipelining and Clocking Styles- Clock Skew and Clock Distribution in Bit-Level Pipelined VLSI Designs- Wave PipeliningConstraint Space Diagram and Degree of Wave Pipelining- Implementation of Wave-Pipelined Systems- Asynchronous Pipelining- Signal Transition Graphs- Use of STG to Design Interconnection Circuits- - Implementation of Computational Units.

UNIT V - LOW POWER VLSI DSP SYSTEMS:

Theoretical Background- Scaling Versus Power Consumption- Power Analysis- Power Reduction Techniques- Power Estimation Approaches.- Simulation Based Approach.

REFERENCES

COURSE OUTCOMES:

- After completing this course the students should be able to:
- Know about the graph representations of DSP algorithms, Convolution algorithms and the concept of parallel recursive and adaptive filters
- Analyze The graph representations of DSP algorithms, Convolution algorithms & concept of parallel recursive and adaptive filters
- Gain the idea of scaling and round off noise and about digital lattice filter structures
- Contribute the knowledge in the design of parallel recursive and adaptive filters
- Demonstrate variable description of digital filters and digital lattice filter structures

***
**COURSE OBJECTIVES:**

- To learn the various limitation on MOSFETS and the alternates.
- To gain knowledge on SET and Carbon nano tubes in the design of transistors
- To learn the basics of molecular electronics and spintronics.

**UNIT I - LIMITATION OF MOSFETS:**

Classical mechanics and its drawbacks, Quantum mechanics, 1D problem - particle in a box, electron tunneling., MOSFET scaling, Non-uniform doping in channel, high K dielectrics, SOI MOSFET, Buried channel MOSFET, Fin FET.

**UNIT II - SINGLE ELECTRONICS:**

Coulomb blockade, Electron tunnelling devices, Single electron transistors , Resonant Tunneling Diodes- principle and applications, Quantum computing, Quantum cellular automata

**UNIT III- CARBON NANO TUBES:**

Carbon nano tubes – Basic structures, CNTFETs, Applications.

**UNIT IV - MOLECULAR ELECTRONICS:**

Molecular wire conductance - Theories of Coherent Electron Transport in molecular junctions, Evaluation of the conductance for coherent transport, Incoherent transport and vibronic coupling, Molecular circuit elements, Circuits.

**UNIT V – SPINTRONICS:**

Spin Vs charge, AMR, GMR, TMR, Spin devices- Spin valves, Magnetic tunnel junctions, Applications – memories (MRAM, STRAM), Logic device, and microwave oscillators.

**REFERENCES:**


**COURSE OUTCOMES:**

After completing this course the students should be able to:

- Understand the fundamental function of cells, and how nanotechnologies interact & Describe the various applications of nanotechnology in biotechnology & medicine with cells.
- Explain the process of self-assembly – from single molecules into nanoparticles
• Describe and explain how nanoparticles are fabricated and characterized & principles of loading small molecule drugs, proteins or nucleic acids (DNA/RNA) into nanoparticles
• Describe and explain the scientific basis and medical benefits for using nanotechnology for treating diseases
• Demonstrate how nanotechnology-based innovation can drive better medicine and a stronger economy

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COURSE OBJECTIVES:

- To explore the various performance measures of RF circuits.
- To acquire knowledge on the design of RF filters, amplifiers and oscillators.

UNIT I - PERFORMANCE PARAMETERS OF RF CIRCUITS:
Gain Parameters, Non-linearity parameters, Noise figure, Phase Noise, Dynamic range, RF front end performance parameters, performance trade offs in an RF circuit.

UNIT II - FILTER DESIGN:
Modern filter design, Frequency and impedance scaling, High Pass filter design, Band pass filter design, Band reject filter design, the effects of finite Q.

UNIT III - HIGH FREQUENCY AMPLIFIER DESIGN:
Zeros as Bandwidth enhances, Shunt-series Amplifier, Bandwidth enhancement with frequency Doublers, Tuned amplifiers, Neutralization and unilateralization, cascaded Amplifiers, LNA Topologies.

UNIT IV - MIXERS AND OSCILLATORS:
Mixer fundamentals, Non linear systems as Linear mixers, multiplier based mixers, Subsampling mixers. Problems with purely linear oscillators, Tuned oscillator, Negative Resistance oscillators, frequency synthesis.

UNIT V - RF POWER AMPLIFIERS:
General considerations, Class A, AB, B & C Power amplifier, Class D, E & F amplifiers, modulation of power amplifiers, RF Power amplifier design examples.

REFERENCES:

COURSE OUTCOMES:
After completing this course the students should be able to:
- Understand the fundamental function of cells, and how nanotechnologies interact & Describe the various applications of nanotechnology in biotechnology & medicine with cells.
- Explain the process of self-assembly – from single molecules into nanoparticles
- Describe and explain how nanoparticles are fabricated and characterized & principles of loading small molecule drugs, proteins or nucleic acids (DNA/RNA) into nanoparticles
- Describe and explain the scientific basis and medical benefits for using nanotechnology for treating diseases
- Demonstrate how nanotechnology-based innovation can drive better medicine and a stronger economy
COURSE OBJECTIVES:

- To understand the concepts of soft computing techniques.
- To enable to develop applications of soft computing in real life problems.

UNIT – I: Fundamentals of Neural Networks & Feed Forward Networks

Basic Concept of Neural Networks, Human Brain, Models of an Artificial Neuron, Learning Methods, Neural Networks Architectures, Signal Layer Feed Forward Neural Network :The Perceptron Model, Multilayer Feed Forward Neural Network :Architecture of a Back Propagation Network(BPN), The Solution, Back propagation Learning, Selection of various Parameters in BPN. Application of Back propagation Networks in Pattern Recognition & Image Processing.

UNIT – II: Associative Memories & ART Neural Networks

Basic concepts of Linear Associator, Basic concepts of Dynamical systems, Mathematical Foundation of Discrete-Time Hop field Networks(HPF), Mathematical Foundation of Gradient-Type Hopfield Networks, Transient response of Continuous Time Networks, Applications of HPF in Solution of Optimization Problem: Minimization of the Traveling salesman tour length, Summing networks with digital outputs, Solving Simultaneous Linear Equations, Bidirectional Associative Memory Networks; Cluster Structure, Vector Quantization, Classical ART Networks, Simplified ART Architecture.

UNIT – III: Fuzzy Logic & Systems

Fuzzy sets, Crisp Relations, Fuzzy Relations, Crisp Logic, Predicate Logic, Fuzzy Logic, Fuzzy Rule based system, Defuzzification Methods, Applications: Greg Viot’s Fuzzy Cruise Controller, Air Conditioner Controller.

UNIT – IV: Genetic Algorithms


UNIT – V: Hybrid Systems


TEXT BOOKS:

1. Introduction to Artificial Neural Systems – J.M.Zurada, Jaico Publishers

REFERENCE BOOKS:

Department of ECE
1. Artificial Neural Networks - Dr. B. Yagananarayana, 1999, PHI, New Delhi.

COURSE OUTCOMES:
After completing this course the students should be able to:
- Understand important and unique engineering issues at microwave and millimeter wave frequency
- Learn microwave network theory and the use of scattering matrix
- Learn design criteria for waveguide and coaxial microwave components.
- Learn the application of these components in the design of useful systems such as radars, receivers, etc.
- Work in small teams and design, fabricate and test a useful microwave component or device, which may be designed using microstripline technology.

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COURSE OBJECTIVES:

- To impart a knowledge on basics of graph theory and its algorithms
- To impart a knowledge on basic optimization techniques.
- To impart a knowledge on various statistical methods in analyzing a sample.

UNIT –I BASICS OF GRAPH THEORY:

UNIT –II CLASSES OF GRAPH:
Eulerian graphs and Hamiltonian graphs - standard theorems-planar graphs-Euler’s formula— five color problem-coloring of graphs-chromatic number (vertex and edge) properties and examples-directed graphs

UNIT –III GRAPH ALGORITHMS:
Computer representation of graphs-Basic graph algorithms— minimal spanning tree algorithm-Kruskal and prim’s algorithm— shortest path algorithms-Dijkstra’s algorithm— DFS and BFS algorithms.

UNIT –IV OPTIMIZATION TECHNIQUES:
Linear programming— graphical methods— simplex method (Artificial variables not included)— transportation and assignment problems.

UNIT –V STATISTICS:
Tchebyshev’s inequality— Maximum likelihood estimation— correlation—partial correlation—multiple correlations— regression— Multiple regressions.

REFERENCES:

COURSE OUTCOMES:
After completing this course the students should be able to:
- Understand the concepts of probability & statics
- Identify the strength and weakness of different theories
- Design and employ appropriate method for solving computing problems
- Analyze and compare the methods.
- Solve computing problems independently.

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VAAGDEVI COLLEGE OF ENGINEERING
(AUTONOMOUS)

(M18SE27) WASTE MANAGEMENT
(Open Elective)

M. Tech:III-Semester

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**COURSE OBJECTIVES:**
- To assess the activities involved for the proposed and determine the type, nature and estimated volumes of waste to be generated.
- To identify any potential environmental impacts from the generation of waste at the site.
- To recommend appropriate waste handling and disposal measures

Unit - I Introduction to Environment:
Ecosystem –meaning- Types -Components- Structure – Functions, Levels of organization in nature- Food chain and Trophic structure, Biogeochemical Cycles, Energy flow.

Unit - II Municipal solid waste:

Unit - III Collection and Transfer Collection:

Unit – IV Processing Techniques and Recovery of Energy:

Unit – V Disposal of Solid Wastes:

**References:**
COURSE OUTCOMES:

- Understand how waste management practices protect environmental health and safety.
- Apply physical and chemical analysis on municipal solid wastes.
- Enhance the route for solid waste collection and transport system.
- Develop a method to use energy from solid wastes.
- Explain different methods of disposal of hazardous solid waste.
VAAGDEVI COLLEGE OF ENGINEERING (AUTONOMOUS)

(M18VL25) DISSERTATION PHASE - I

M. Tech: III-Semester

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COURSE OUTCOMES:

After the completion of this course, the students should be able to

- In Master’s Project Phase-I, the students should select a recent topic from a reputed International Journal, preferably IEEE, ACM, Springer in the field that has direct or indirect relation to the area of specialization.
- After conducting a detailed literature survey, they should compare and analyze research work done and review recent developments in the area and prepare an initial design of the work to be carried out as Master’s Project.
- It is mandatory that the students should refer National and International Journals and conference proceedings while selecting a topic for their Project.
- Emphasis should be given for introduction to the topic, literature survey, and scope of the proposed work along with some preliminary work carried out on the Project topic. Students should submit a copy of Phase-I Project report covering the content discussed above and highlighting the features of work to be carried out in Phase-II of the Project.

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VAAGDEVI COLLEGE OF ENGINEERING
(AUTONOMOUS)

(M18VL26) DISSERTATION PHASE - II

M. Tech: IV-Semester

COURSE OUTCOMES:

After the completion of this course, the students should be able to

- Use Specialized knowledge and skills in engineering and apply it effectively on a project.
- Apply knowledge of the ‘real world’ situations that a professional engineer can encounter.
- Apply critical and creative thinking in the design of VLSI System Design projects.
- Demonstrate a sound technical knowledge of selected project topic.
- Demonstrate the skills and attitude of a professional engineer.
- Summarize an appropriate list of literature review, analyse previous work and relate them to current project.
- Deliver technical seminar based on the Project work carried out.
- Publish the conducted research work in a National / International Conference or Journal preferably IEEE, ACM, Springer and Scopus indexed/SC Indexed/ESCI.