COURSE STRUCTURE AND DETAILED SYLLABUS

M.TECH
VLSI SYSTEM DESIGN

For
M.TECH TWO YEAR DEGREE PROGRAMME
(Applicable for the batches admitted from 2018-2019)

VAAGDEVI COLLEGE OF ENGINEERING
(Autonomous)
Bollikunta, Warangal-506 005
Telangana State, India.

VAAGDEVI COLLEGE OF ENGINEERING

Autonomous
Bollikunta, Warangal

Department of Electronics & Communication Engineering

M.TECH. (VLSI System Design)

COURSE STRUCTURE

(R18 Regulations applicable for the batches admitted from Academic Year 2018-19 onwards)

I-SEMESTER

S.No.	Course Code	Title of the Course	L	T	P	Credits
1	M18VL01	CMOS Digital Integrated Circuit Design	3	0	0	3
2	M18VL02	CMOS Analog Integrated Circuit Design	3	0	0	3
3	M18VL03 M18VL04 M18VL05	**Program Elective-I** Digital System Design using HDL VLSI Signal Processing VLSI Technology	3	0	0	3
4	M18VL06 M18VL07 M18VL08	**Program Elective-II** Algorithms For VLSI Design Automation Embedded System Design Device Modelling	3	0	0	3
5	M18AC01	English For Research Paper Writing	2	0	0	0
6	M18MC01	Research Methodology	2	0	0	2
7	M18VL09	HDL Programming Laboratory	0	0	4	2
8	M18VL10	Digital IC Design Laboratory	0	0	4	2
		Total Credits	**16**	**00**	**08**	**18**

II-SEMESTER

S.No.	Course Code	Title of the Course	L	T	P	Credits
1	M18VL11	CMOS Mixed Signal Circuit Design	3	0	0	3
2	M18VL12	VLSI Design Verification and Testing	3	0	0	3
3	M18VL13 M18VL14 M18VL15	**Program Elective-III** Low Power VLSI Design Optimization Technique In VLSI Design High Speed VLSI Design	3	0	0	3
4	M18VL16 M18VL17 M18VL18	**Program Elective-IV** ASIC Design System On Chip Architecture Semiconductor Memory Design & Testing	3	0	0	3
5	M18AC02	Stress Management	2	0	0	0
6	M18VL19	Analog IC Design Laboratory	0	0	4	2
7	M18VL20	Mixed Signal VLSI Laboratory	0	0	4	2
8	M18VL21	Mini Project	0	0	4	2
		Total Credits	**14**	**00**	**12**	**18**

VAAGDEVI COLLEGE OF ENGINEERING

Autonomous
Bollikunta, Warangal

Department of Electronics & Communication Engineering

M.TECH. (VLSI System Design)

COURSE STRUCTURE

(R18 Regulations applicable for the batches admitted from Academic Year 2018-19 onwards)

III-SEMESTER

S.No.	Course Code	Title of the Course	L	T	P	Credits
1		**Program Elective-V**	3	0	0	3
	M18VL22	High Speed VLSI Architectures for DSP Applications				
	M18VL23	Nano materials & Nano Technology				
	M18VL24	RF Circuit Design				
2		**Open Elective**	3	0	0	3
	M18CS12	Soft Computing Techniques				
	M18MA02	Graph Theory & Optimization Techniques				
	M18SE27	Waste Management				
3	M18VL25	Dissertation Phase-I	0	0	20	10
		Total Credits	**06**	**00**	**20**	**16**

IV-SEMESTER

S.No.	Course Code	Title of the Course	L	T	P	Credits
1	M18VL26	Dissertation Phase-II	0	0	32	16
		Total Credits	**00**	**00**	**32**	**16**

****

VAAGDEVI COLLEGE OF ENGINEERING
(AUTONOMOUS)

(M18VL01) CMOS DIGITAL INTEGRATED CIRCUIT DESIGN

M. Tech: I- Semester **L T P C**
3 0 0 3

UNIT –I:
MOS Design
Pseudo NMOS Logic – Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

UNIT –II:
Combinational MOS Logic Circuits:
MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, Complex Logic circuits design – Realizing Boolean expressions using NMOS gates and CMOS gates , AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

UNIT –III:
Sequential MOS Logic Circuits:
Behavior of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flipflop.

UNIT –IV:
Dynamic Logic Circuits:
Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

UNIT –V:
Semiconductor Memories:
Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory- NOR flash and NAND flash.

TEXT BOOKS:
1. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

REFERENCE BOOKS:
1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Digital Integrated Circuits – A Design Perspective, Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, 2nd Ed., PHI.

COURSE OUTCOMES:
After the completion of this course, the students should be able to
- Define the basic of CMOS technology
- Relate, compare, interpret and make the use of the best CMOS design techniques for

implementation, analysis & design of Combinational MOS logic circuits

- Know & tell different types of memories and compare performance evaluation of each memory modules so they can be able to think & justify how to improve performance by taking different structures.
- Define, simplify & justify which dynamic logic circuit can be used investigate CMOS circuits.
- Recommend various CMOS techniques and also other device technologies based on circuit constraints requirement.

***

VAAGDEVI COLLEGE OF ENGINEERING
(AUTONOMOUS)

(M18VL02) CMOS ANALOG INTEGRATED CIRCUIT DESIGN

M. Tech: I-Semester **L T P C**
3 0 0 3

COURSE OBJECTIVES:
- To understand the fundamentals of IC technology.
- To understand the analysis and design of analog integrated circuits starting from basic building blocks to different implementations of the amplifiers in CMOS technology.

UNIT –I:
MOS Devices and Modeling
The MOS Transistor, Passive Components- Capacitor & Resistor, Integrated circuit Layout, CMOS Device Modeling – Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

UNIT –II:
Analog CMOS Sub-Circuits:
MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

UNIT –III:
CMOS Amplifiers:
Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain, Amplifiers Architectures.

UNIT –IV:
CMOS Operational Amplifiers:
Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power-Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of OP Amp.

UNIT –V:
Comparators:
Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop-Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

TEXT BOOKS:
1. CMOS Analog Circuit Design – Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
2. Analysis and Design of Analog Integrated Circuits- Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer, Wiley India, Fifth Edition, 2010.

REFERENCE BOOKS:
1. Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edn, 2013. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition.
2. CMOS: Circuit Design, Layout and Simulation- Baker, Li and Boyce, PHI.

COURSE OUTCOMES:
Upon completion of this course, students should demonstrate the ability to:

- Define the parameters of MOS Devices & can predict the performance or behavior of Analog VLSI circuit.
- Use mathematical models of MOS transistors to evaluate their behavior in analog circuits & selects suitable design approaches while trading off conflicting requirements
- Analyze & characterize analog devices and systems & Designing CMOS analog circuits to achieve performance specifications
- Understand design issues related to analog VLSI system 7&working of MOS based data converter circuits.
- Make the significant use of knowledge of subject in research or on project in VLSI domain.

***

VAAGDEVI COLLEGE OF ENGINEERING
(AUTONOMOUS)
(M18VL03) DIGITAL SYSTEM DESIGN USING HDL
(Program Elective – I)

M. Tech: I-Semester **L T P C**
3 0 0 3

COURSE OBJECTIVES:

- To understand the different abstract levels in Verilog for modeling digital circuits.
- The student will learn the basic CMOS circuit, characteristics and performance.
- The student will learn the designing of combinational and sequential circuits in CMOS.

UNIT I - BASIC CONCEPTS - VERILOG

Operators, Basic concepts, Identifiers, System task and functions, Value set, Data types, Parameters, Operands, Operators, Modules and ports, Gate-level Modeling, Dataflow Modeling, Behavioral Modeling, Switch level modeling, Tri state gates, MOS Switches, Bidirectional switches, User defined primitives, Combinational UDP, Sequential UDP. Introduction to synthesis, Verilog HDL synthesis-Synthesis Design flow Test bench-lab exercise.

UNIT II – BASICS OF MOS TRANISTORS

MOS transistors- Threshold voltage- characteristics of MOS transistorchannel length modulation- short channel effects- Design of Logic gates using NMOS, PMOS and CMOS, Stick diagrams- Transfer characteristics of CMOS inverter- Power dissipation – Delay and sizing of inverters- Lab exercise.

UNIT III - CMOS – COMBINATIONAL CIRCUITS

Static CMOS design-complementary CMOS - static propertiescomplementary CMOS design-Power consumption in CMOS logic gatesdynamic or glitching transitions - Design techniques to reduce switching activity - Radioed logic-DC VSL - pass transistor logic - Differential pass transistor logic -Sizing of level restorer-Sizing in pass transistor-Dynamic CMOS design-Basic principles - Domino logic-optimization of Domino logic-NPCMOS-logic style selection - Designing logic for reduced supply voltages. Lab exercise in Switch level modeling.

UNIT IV - CMOS – SEQUENTIAL CIRCUITS

Timing metrics for sequential circuit - latches Vs registers -static latches and registers - Bistability principle - multiplexer based latches-master slave edge triggered registers- non-ideal clock signals-low voltage static latches-static SR flip flop - Dynamic latches and registers-C2MOS register - Dual edge registers-True single phase clocked registers-pipelining to optimize sequential circuit latch Vs register based pipelines-non-Bistable sequential circuit-Schmitt trigger-mono stable -Astable -sequential circuit - choosing a clocking strategy.. Lab exercise in Switch level modeling

UNIT V – SUB-SYSTEM DESIGN/ SYSTEM VERILOG

Addition/Subtraction - Comparators- Zero/One Detectors- Binary Counters- ALUs Multiplication- Shifters- Memory elements- control: Finite-State Machines. Lab exercise.

REFERENCES

1. Samir palnitkar, ”Verilog HDL”, Pearson education, Second Edition,20O3.
2. J. Bhasker, “A Verilog HDL Primer”, Second Edition, Star Galaxy, 2005.
3. J. Bhasker, “A Verilog Synthesis: A Practical Primer”, Star Galaxy, 1998
4. Jan.M.Rabaey., Anitha Chandrakasan Borivoje Nikolic, "DigitalIntegrated Circuits", Second Edition
5. Neil H.E Weste and Kamran Eshraghian, "Principles of CMOS VLSI Design", 2nd Edition Addition ,Wesley, 1998.,

COURSE OUTCOMES:
Upon completion of this course, students should demonstrate the ability to:

- Design and analyze combinational, sequential and arithmetic circuits using HDL.
- Understand digital system design flow, timing, synthesis and FPGA implementation issues.
- Solve engineering problems in the area of digital system design & Examine or Inspect for an optimum layout for IC layout at VLSI backend design.
- Design, analyze & can predict the performance characteristics of logic gates using NMOS, PMOS & CMOS technology at VLSI backend design.
- Tell an optimum trade with respect to three basic parameters of VLSI design for VLSI circuit at frontend or backend VLSI design

***

VAAGDEVI COLLEGE OF ENGINEERING
(AUTONOMOUS)

(M18VL04)VLSI SIGNAL PROCESSING
(Program Elective – I)

M. Tech: I-Semester **L T P C**
3 0 0 3

COURSE OBJECTIVES:
- To understand the fundamentals of DSP
- To learn various DSP structures and their implementation.
- To know designing constraints of various filters.

UNIT I - INTRODUCTION TO DIGITAL SIGNAL PROCESSING:
Linear System Theory- Convolution- Correlation - DFT- FFT- Basic concepts in FIR Filters and IIR Filters- Filter Realizations. Representation of DSP Algorithms-Block diagram-SFG-DFG.

UNIT II - ITERATION BOUND, PIPELINING AND PARALLEL PROCESSING OF FIR FILTER:
Data-Flow Graph Representations- Loop Bound and Iteration BoundAlgorithms for Computing Iteration Bound-LPM Algorithm. Pipelining and Parallel Processing: Pipelining of FIR Digital Filters- Parallel ProcessingPipelining and Parallel Processing for Low Power. Retiming: DefinitionsProperties and problems- Solving Systems of Inequalities.

UNIT III - FAST CONVOLUTION AND ARITHMETIC STRENGTH REDUCTION IN FILTERS:
Cook-Toom Algorithm- Modified Cook-Toom Algorithm.Design of Fast Convolution Algorithm by Inspection. Parallel FIR filters-Fast FIR algorithms-Two parallel and three parallel. Parallel architectures for Rank Order filters-Odd Even Merge sort architecture-Rank Order filter architecture-Parallel Rank Order filters-Running Order Merge Order SorterLow power Rank Order filter.

UNIT IV - PIPELINED AND PARALLEL RECURSIVE FILTERS:
Pipeline Interleaving in Digital Filters- Pipelining in 1st Order IIR Digital Filters- Pipelining in Higher- Order IIR Filters-Clustered Look ahead and Stable Clustered Look ahead- Parallel Processing for IIR Filters and Problems.

UNIT V - SCALING AND ROUNDOFF NOISE: Introduction to Scaling and Roundoff Noise- State Variable Description of Digital Filters- Scaling and Roundoff Noise Computation- Round Off Noise Computation Using State Variable Description- Slow-Down- Retiming and Pipelining.

REFERENCES

1. K.K Parhi: "VLSI Digital Signal processing", John-wiley, 2nd Edition Reprint, 2008.
2. John G.Proakis, Dimitris G.Manolakis, "Digital Signal Processing", Prentice Hall of India, 1st Edition, 2009.

COURSE OUTCOMES:
Upon completion of this course, students should demonstrate the ability to:

- Apply the concepts of pipelining, parallel processing, retiming, folding and unfolding to optimize digital signal processing architectures
- Use of proper techniques for parallel processing design for scaling and round off noise

computation

- Apply all techniques to improve implementations of several DSP algorithms, using both ASICs and off –the -shelf programmable digital signal processors
- Design high-speed, low-area, and low-power VLSI systems for a broad range of DSP applications
- Minimize the computational complexity using fast convolution algorithms & Make the significant use of knowledge of subject in research or on project in VLSI domain

***

VAAGDEVI COLLEGE OF ENGINEERING
(AUTONOMOUS)

(M18VL05)VLSI TECHNOLOGY
(Program Elective – I)

M. Tech:I-Semester **L T P C**
3 0 0 3

COURSE OBJECTIVES:

- To understand the impact of the physical and chemical processes of integrated circuit fabrication technology on the design of integrated circuits.
- To understand physics of the Crystal growth, wafer fabrication and basic properties of silicon wafers.
- To Learn the concepts of Design rules and Scaling, BICMOS ICs.

UNIT –I:

Review of Microelectronics and Introduction to MOS Technologies:

MOS, CMOS, BiCMOS Technology. Basic Electrical Properties of MOS, CMOS & BiCMOS Circuits: Ids – Vds relationships, Threshold Voltage VT, Gm, Gds and ωo, Pass Transistor, MOS, CMOS & Bi CMOS Inverters, Zpu/Zpd, MOS Transistor circuit model, Latch-up in CMOS circuits.

UNIT –II:

Layout Design and Tools:

Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools. Logic Gates & Layouts:Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and Inductive interconnect delays.

UNIT –III:

Overview of semiconductor industry, Stages of Manufacturing, Process and product trends, Crystal growth, Basic wafer fabrication operations, process yields, Semiconductor material preparation, Basic wafer fabrication operations, Yield measurement, Contamination sources, Clean room construction, Oxidation and Photolithography, Doping and Depositions, Metallization.Ten step patterning process, Photoresists, physical properties of photoresists, Storage and control of photoresists, photo masking process, Hard bake, develop inspect, Dry etching Wet etching, resist stripping

UNIT –IV

Doping and depositions: Diffusion process steps, deposition, Drive-in oxidation, Ion implantation-1, Ion implantation-2, CVD basics, CVD process steps, Low pressure CVD systems, Plasma enhanced CVD systems, Vapour phase epitoxy, molecular beam epitaxy.

UNIT –V

Design rules and Scaling, BICMOS ICs: Choice of transistor types, pnp transistors, Resistors, capacitors, Packaging: Chip characteristics, package functions, package operations

TEXT BOOKS:

1. Peter Van Zant, Microchip fabrication, McGraw Hill, 1997.
2. C.Y. Chang and S.M. Sze, ULSI technology, McGraw Hill, 2000

REFERENCE BOOKS:

1. Micro Electronics circuits Analysis and Design 2nd Edition, Muhammad H Rashid, CENAGE Learning2011.
2. Eugene D. Fabricius, Introduction to VLSI design, McGraw Hill, 1999

3. Wani-Kai Chen (editor), The VLSI Hand book, CRI/IEEE press, 2000
4. S.K. Gandhi, VLSI Fabrication principles, John Wiley and Sons, NY, 1994

COURSE OUTCOMES:

Upon completion of this course, students should demonstrate the ability to:

- Build circuits using IC's.
- In depth knowledge of applying the concepts in real time applications.
- Understand the main elements of hierarchical IC design namely interested circuit technology, approaches to system design, architectural issues.
- Design implementation and layout & Use of tools for efficient designing.
- Make the significant use of knowledge of subject in research or on project in VLSI domain.

***

VAAGDEVI COLLEGE OF ENGINEERING
(AUTONOMOUS)

(M18VL06)ALGORITHMS FOR VLSI DESIGN AUTOMATION
(Program Elective – II)

M. Tech:I-Semester **L T P C**
3 0 0 3

COURSE OBJECTIVES:
- Understand the concepts of Physical Design Process such as partitioning, Floorplanning, Placement and Routing.
- Discuss the concepts of design optimization algorithms and their application to physical design automation.
- Understand the concepts of simulation and synthesis in VLSI Design Automation
- Formulate CAD design problems using algorithmic methods.

UNIT I:
PRELIMINARIES
Introduction to Design Methodologies, Design Automation tools, Algorithmic Graph Theory, Computational complexity, Tractable and Intractable problems.

UNIT II:
GENERAL PURPOSE METHODS FOR COMBINATIONAL OPTIMIZATION
Backtracking, Branch and Bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu search, Genetic Algorithms.

UNIT III:
LAYOUT COMPACTION, PLACEMENT, FLOORPLANNING AND ROUTING
Problems, Concepts and Algorithms.
MODELLING AND SIMULATION
Gate Level Modelling and Simulation, Switch level Modelling and Simulation.

UNIT IV:
LOGIC SYNTHESIS AND VERIFICATION
Basic issues and Terminology, Binary-Decision diagrams, Two-Level logic Synthesis
HIGH-LEVEL SYNTHESIS
Hardware Models, Internal representation of the input Algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithms, Some aspects of Assignment problem, High-level Transformations.

UNIT V:
PHYSICAL DESIGN AUTOMATION OF FPGAs
FPGA technologies, Physical Design cycle for FPGAs, partitioning and Routing for segmented and staggered Models.

PHYSICAL DESIGN AUTOMATION OF MCMs
MCM technologies, MCM physical design cycle, Partitioning, Placement - Chip Array based and Full Custom Approaches, Routing – Maze routing, Multiple stage routing, Topologic routing, Integrated Pin – Distribution and routing, Routing and Programmable MCMs.

TEXT BOOKS

1. Algorithms for VLSI Design Automation, S.H. Gerez, 1999, WILEY Student Edition, John wiley & Sons (Asia) Pvt. Ltd.
2. Algorithms for VLSI Physical Design Automation – Naveed Sherwani, 3rd Ed., 2005, Springer International Edition.

REFERENCE BOOKS

1. Computer Aided Logical Design with Emphasis on VLSI – Hill & Peterson, 1993, Wiley.
2. Modern VLSI Design: Systems on silicon – Wayne Wolf, 2nd ed., 1998, Pearson Education Asia.

COURSE OUTCOMES:

Upon completion of this course, students should demonstrate the ability to:

- Describe and formulate the flow of VLSI Design for any application.
- Explain the algorithms for partitioning, floor planning, placement and routing the digital designs at frontend level & at backend VLSI Design level.
- Compare the various scheduling algorithms & Analyze & solve the issues related to logic synthesis & verification
- Explain the algorithms for partitioning, floor planning, placement and routing the MCM modules
- Make significant contribution in the research in based on design of CAD tool for VLSI design

***

VAAGDEVI COLLEGE OF ENGINEERING
(AUTONOMOUS)

(M18VL07)EMBEDDED SYSTEM DESIGN
(Program Elective – II)

M. Tech:I-Semester **L T P C**
3 0 0 3

COURSE OBJECTIVES:
- To introduce students to the modern embedded systems and to show how to understand and program such systems using a concrete platform built around A modern embedded processor like the Intel ATOM.
- To introduce the students to Embedded Firmware.
- To understand the concepts of RTOS based Embedded design.

UNIT –I:
Introduction to Embedded Systems
Definition of Embedded System, Embedded Systems Vs General Computing Systems, History of Embedded Systems, Classification, Major Application Areas, Purpose of Embedded Systems, Characteristics and Quality Attributes of Embedded Systems.

UNIT –II:
Typical Embedded System:
Core of the Embedded System: General Purpose and Domain Specific Processors, ASICs, PLDs, Commercial Off-The-Shelf Components (COTS), Memory: ROM, RAM, Memory according to the type of Interface, Memory Shadowing, Memory selection for Embedded Systems, Sensors and Actuators, Communication Interface: Onboard and External Communication Interfaces.

UNIT –III:
Embedded Firmware:
Reset Circuit, Brown-out Protection Circuit, Oscillator Unit, Real Time Clock, Watchdog Timer, Embedded Firmware Design Approaches and Development Languages.

UNIT –IV:
RTOS Based Embedded System Design:
Operating System Basics, Types of Operating Systems, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling.

UNIT –V:
Task Communication: Shared Memory, Message Passing, Remote Procedure Call and Sockets, Task Synchronization: Task Communication/Synchronization Issues, Task Synchronization Techniques, Device Drivers, How to Choose an RTOS.

TEXT BOOKS:
1. Introduction to Embedded Systems – Shibu K.V, Mc Graw Hill.

REFERENCE BOOKS:
1. Embedded Systems – Raj Kamal, TMH.
2. Embedded System Design – Frank Vahid, Tony Givargis, John Wiley.
3. Embedded Systems – Lyla, Pearson, 2013
4. An Embedded Software Primer – David E. Simon, Pearson Education.

COURSE OUTCOMES:
Upon completion of this course, students should demonstrate the ability to:

.

- Know the Basic Concept of Embedded Systems.
- Interpret the difference between Microcontrollers and Microprocessors.
- Apply the Software for Embedded System Design & concepts of Embedded OS.
- Explain and apply the concept of Embedded Firmware, RTOS Based Embedded System Design and Task function.
- Make significant contribution in the research in applications based on embedded system design.

***

VAAGDEVI COLLEGE OF ENGINEERING
(AUTONOMOUS)

(M18VL08)DEVICE MODELLING
(Program Elective – II)

M. Tech:I-Semester **L T P C**
3 0 0 3

COURSE OBJECTIVES:
- To make the student understand how MOSFET and other semiconductor devices are modeled
- To impart knowledge to simulate MOSFET for various operational requirements.
- To impart a knowledge on advanced structures of MOSFETs like SOIFET, FinFET etc.

UNIT -I:
Introduction to Semiconductor Physics:
Review of Quantum Mechanics, Boltzman transport equation, Continuity equation, Poisson equation.
Integrated Passive Devices:
Types and Structures of resistors and capacitors in monolithic technology, Dependence of model parameters on structures

UNIT -II: Integrated Diodes:
Junction and Schottky diodes in monolithic technologies – Static and Dynamic behavior – Small and large signal models – SPICE models
Integrated Bipolar Transistor:
Types and structures in monolithic technologies – Basic model (Eber-Moll) – Gunmel - Poon model-dynamic model, Parasitic effects – SPICE model –Parameter extraction

UNIT -III:
Integrated MOS Transistor:
NMOS and PMOS transistor – Threshold voltage – Threshold voltage equations – MOS device equations – Basic DC equations second order effects – MOS models – small signal AC characteristics – MOS FET SPICE model level 1, 2, 3 and 4

UNIT -IV:
VLSI Fabrication Techniques: An overview of wafer fabrication, Wafer Processing – Oxidation – Patterning – Diffusion – Ion Implantation – Deposition – Silicon gate nMOS process – CMOS processes – n-well- p-well- twin tub- Silicon on insulator – CMOS process enhancements – Interconnects circuit elements

UNIT -V:
Modeling of Hetero Junction Devices: Band gap Engineering, Band gap Offset at abrupt Hetero Junction, Modified current continuity equations, Hetero Junction bipolar transistors (HBTs), SiGe

TEXT BOOKS:
1. Introduction to Semiconductor Materials and Devices – Tyagi M. S, 2008, John Wiley Student Edition.
2. Solid State Circuits – Ben G. Streetman, Prentice Hall, 1997

REFERENCE BOOKS:
1. Physics of Semiconductor Devices – Sze S. M, 2nd Edition, Mcgraw Hill, New York, 1981.
2. Introduction to Device Modeling and Circuit Simulation – Tor A. Fijedly, Wiley-

Interscience, 1997.
3. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011

COURSE OUTCOMES:

Upon completion of this course, students should demonstrate the ability to:

- Understand the physics of and design elements of silicon MOSFETs.
- Explain the equations, approximations and techniques available for deriving a model with specified properties, for a general device characteristic with known qualitative theory
- Analyze the performance issues & inherent trade off involved in system design Offer clues to qualitative understanding of the physics of a new device and conversion of this understanding into equations.
- Utilize semiconductor models to analyze carrier densities and carrier transport & Simulate characteristics of a simple device using MATLAB, SPICE and SYNOPSYS
- Understand and analyze the inner working of semiconductor p-n diodes, Schottky barrier diodes and advanced MOSFET technology

***

VAAGDEVI COLLEGE OF ENGINEERING
(AUTONOMOUS)

(M18AC01)ENGLISH FOR RESEARCH PAPER WRITING

M. Tech:I-Semester **L T P C**
2 0 0 0

Course Objectives:

- To understand the nuances of language and vocabulary in writing a Research Paper.
- To develop the content, structure and format of writing a research paper.
- To give the practice of writing a Research Paper.
- To enable the students to evolve original research papers without subjected to plagiarism.

UNIT I:

ACADEMIC WRITING: What is Research? - Meaning & Definition of a research paper– Purpose of a research paper – Scope – Benefits – Limitations – outcomes.

UNIT II:

RESEARCH FORMAT: Title – Abstract – Introduction – Discussion - Findings – Conclusion – Style of Indentation – Font size/Font types – Indexing – Citation of sources.

UNIT III:

RESEARCH METHODOLOGY: Methods (Qualitative – Quantitative) – Literature Review – Who did what – Criticizing, Paraphrasing & Plagiarism.

UNIT IV:

PROCESS OF WRITING A RESEARCH PAPER: Choosing a topic - Thesis Statement – Outline – Organizing notes - Language of Research – Word order, Paragraphs – Writing first draft –Revising/Editing - Typing the final draft

UNIT V:

HOW TO & WHERE TO GET PUBLISHED: Reputed Journals – National/International – ISSN No, No. of volumes, Scopes Index/UGC Journals – Free publications - Paid Journal publications – /Advantages/Benefits

TEXT BOOKS:

1. MLA Hand book for writers of Research Papers, East West Press Pvt. Ltd, New Delhi, 7th Edition.
2. C. R Kothari, Gaurav, Garg, Research Methodology Methods and Techniques, New Age International Publishers. 4th Edition.
3. Lauri Rozakis, Schaum's Quick Guide to Writing Great Research Papers, Tata McGraw Hills Pvt. Ltd, New Delhi.
4. N. Gurumani, Scientific Thesis Writing and Paper Presentation, MJP Publishers

REFERENCES:

1. NPTEL: https://onlinecourses.nptel.ac.in/noc18_mg13/preview

COURSE OUTCOMES:

- Upon completion of this course, students should demonstrate the ability to:

- Understand the nuances of language and vocabulary in writing a Research Paper
- Develop the content, structure and format of writing a research paper
- Analyze and practice writing a Research Paper
- Enable the students to plan for original research papers without subjected to plagiarism.

****

VAAGDEVI COLLEGE OF ENGINEERING
(AUTONOMOUS)

(M18MC01)RESEARCH METHODOLOGY

M. Tech: I-Semester **L T P C**
2 0 0 2

Course Objectives:

- To develop an understanding of IPR/ research methodology in the process of creation of patents through research.
- To develop further research capabilities.
- To learn better report writing skills and Patenting.

UNIT I:

RESEARCH METHODOLOGY: Objectives and Motivation of Research, Significance of Literature review, Types of Research, Research Approaches, and Research Methods verses Methodology, Research and Scientific Method, Importance of Research Methodology, Research Process, Criteria of Good Research.

UNIT II:

RESEARCH DESIGN: Meaning of Research Design, Need of Research Design, Feature of a Good Design Important Concepts Related to Research Design, Different Research Designs, Basic Principles of Experimental Design, Data collection methods, Collection of primary data, Secondary data, Data organization, Methods of data grouping, Diagrammatic representation of data, Graphic representation of data.

UNIT III:

RESEARCH REPORT WRITING: Format of the Research report, Synopsis, Dissertation, References/Bibliography/ Webliography, Research Proposal Preparation: Writing a Research Proposal and Research Report, Writing Research Grant Proposal.

UNIT IV:

NATURE OF INTELLECTUAL PROPERTY: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development.

UNIT V:

PATENT RIGHTS: Scope of Patent Rights. Licensing and transfer of technology. Patentinformation and databases. New Developments in IPR: Administration of Patent System.

TEXT BOOKS:

1. C.R Kothari, "Research Methodology, Methods & Technique". New Age International Publishers, 2004.
2. R. Ganesan, "Research Methodology for Engineers", MJP Publishers, 2011.
3. Robert P. Merges, Peter S. Menell, Mark A. Lemley, "Intellectual Property in New Technological Age", Aspen Publishers, 2016.
4. T. Ramappa, "Intellectual Property Rights Under WTO", S. Chand, 2008.
5. Satarkar, S.V,."Intellectual property rights and copy right". ESS Publications, 2000.

REFERENCES:

1. Ranjit Kumar, "Research Methodology: A Step by Step Guide for beginners", SAGE Publications Ltd.
2. Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd ,2007

COURSE OUTCOMES:

- Upon completion of this course, students should demonstrate the ability :
- Develop an understanding of IPR/ research methodology in the process of creation of patents through research
- Develop further research capabilities
- Design Important Concepts Related to Research Design
- Learn better report writing skills and Patenting.

***

VAAGDEVI COLLEGE OF ENGINEERING
(AUTONOMOUS)

(M18VL09)HDL PROGRAMMING LABORATORY

M. Tech:I-Semester **L T P C**
0 0 4 2

Note: Any 10 of the following digital/analog circuits are to be designed and implemented using Xilinx/Altera/Equivalent CAD tools.

Programming can be done using any complier. Down load the programs on FPGA/CPLD boards and performance testing may be done apart from verification by simulation with any of the front end tools.

COURSE OBJECTIVES:
- To design Various Combinational and Sequential circuits using VHDL
- To design Various Combinational and Sequential circuits using Verilog HDL.
- To verify different logic circuits using FPGA/CPLD Boards.

List of Experiments:

1. Design and Simulate Combinational circuits in all three modeling of VHDL
2. Design and Simulate 4-bit adder in structural and behavioral modeling VHDL
3. Design and Simulate sequential circuits using VHDL.
4. Design and Simulate State machine using VHDL.
5. Design and Simulate Traffic Light Controller using VHDL.
6. Design and simulation of combinational circuit test bench.
7. Design and Simulate ALU using Packages and user defined data type.
8. Design and Simulate Flip-flops using VHDL
9. Design and Simulate Combinational circuits using Verilog HDL
10. Design and Simulate Sequential circuits using Verilog HDL
11. Design and Simulate logic gates using Switch level modeling
12. FPGA implementation of combinational circuit using VHDL and Verilog HDL

COURSE OUTCOMES:
Upon completion of this course, students should demonstrate the ability :

- Apply the knowledge in Simulation and Synthesis of Digital Circuits.
- Design Various Combinational and Sequential circuits using Verilog HDL & HDL
- Explain the System Modeling with Tasks and Functions.
- Design of digital circuits using FPGA/CPLD boards.

***

VAAGDEVI COLLEGE OF ENGINEERING
(AUTONOMOUS)

(M18VL10)DIGITAL IC DESIGN LABORATORY

M. Tech:I-Semester **L T P C**
0 0 4 2

Note: Any 10 of the following digital/analog circuits are to be designed and implemented using Mentor Graphics / Tanner Tools/Microwind-DSCH/Equivalent CAD tools.

COURSE OBJECTIVES:

- To design Various Combinational circuits using CMOS Logic.
- To design Various Sequential circuits using CMOS Logic.
- To design Various circuits using Different Logic Styles.
- To design Layout of Different logic circuits.

List of Experiments:

1. Design and Simulation of CMOS/NMOS Inverter.
2. Design and Simulation of CMOS Universal Gates.
3. Design and Simulation of Full Adder and Full Subtractor.
4. Design and Simulation of Domino Logic and NORA Logic.
5. Design and Simulation of Dynamic Logic and Pseudo NMOS Logic.
6. Design and Simulation of Transmission Gate and Pass Transistor Logic.
7. Design and Simulation of Bi-CMOS Inverter.
8. Design and Simulation of Bi-CMOS NAND/NOR Logic.
9. Design and Simulation of SRAM Design.
10. Design and Simulation DRAM Design.
11. Post Layout Simulation CMOS Inverter.
12. Post Layout Simulation of CMOS Universal Gates.
13. Post Layout Simulation of Combinational Circuits.

COURSE OUTCOMES:

- Design CMOS inverters, logic circuits and transmission gates to specifications.
- Design latches and flip-flops asthe basic circuit for Random-Access- Memory (RAM) and Read-Only-Memory (ROM) cells.
- Understand the Design of Bi-CMOS Inverter, logic circuits.
- Design post Layout of Different logic circuits.

***

VAAGDEVI COLLEGE OF ENGINEERING
(AUTONOMOUS)

(M18VL11)CMOS MIXED SIGNAL CIRCUIT DESIGN

M. Tech:II-Semester **L T P C**
3 0 0 3

COURSE OBJECTIVES:
- To know mixed signal circuits like DAC, ADC, PLL etc.
- To gain knowledge on filter design in mixed signal mode.
- To acquire knowledge on design different architectures in mixed signal mode.

UNIT -I:
Switched Capacitor Circuits:
Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing, biquad filters.

UNIT -II:
Phased Lock Loop (PLL):
Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs-PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications

UNIT -III:
Data Converter Fundamentals:
DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters

UNIT -IV:
Nyquist Rate A/D Converters:
Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Time interleaved converters.

UNIT -V:
Oversampling Converters:
Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multibit quantizers, Delta sigma D/A

TEXT BOOKS:
1. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition, 2002
2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
3. Analog Integrated Circuit Design- David A. Johns,Ken Martin, Wiley Student Edition, 2013

REFERENCE BOOKS:
1. CMOS Integrated Analog-to- Digital and Digital-to-Analog converters-Rudy Van De Plassche, Kluwer Academic Publishers, 2003
2. Understanding Delta-Sigma Data converters-Richard Schreier, Wiley Interscience, 2005.
3. CMOS Mixed-Signal Circuit Design – R. Jacob Baker, Wiley Interscience, 2009.

COURSE OUTCOMES:

After completing this course the students should be able to:

- Build mixed signal circuits like DAC, ADC, PLL etc &Gain knowledge on filter design in mixed signal mode &To acquire knowledge on design different architectures in mixed signal mode.
- Analyze digital test and linear test engineers to the mixed signal world by teaching the basics of analog and mixed signal test methods. Sampling Theory, Frequency Domain Testing, and Digital Signal Processing
- Apply these fundamental concepts to different test methods and data validation for mixed signal parameters together with debugging, noise reduction and device interface techniques.
- Deal with the theory and design skills of CMOS op-amps, voltage reference circuits, switched capacitor circuits, sample-and- hold circuits, and A/D & D/A converters used in modern communication systems and consumer electronic products.
- Design of core mixed-signal IC blocks: comparators and data converters & System level design flow: top-down and bottom-up design methodologies

***

VAAGDEVI COLLEGE OF ENGINEERING
(AUTONOMOUS)

(M18VL12)VLSI DESIGN VERIFICATION AND TESTING

M. Tech:II-Semester **L T P C**
3 0 0 3

COURSE OBJECTIVES:
- To gain knowledge on digital testing as applied to VLSI design.
- To acquire knowledge on testing of algorithms for digital circuits.
- To learn various testing methods for digital circuits.

UNIT -I:
Introduction to Testing:
Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

UNIT -II:
Logic and Fault Simulation:
Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation, ATPG.

UNIT -III:
Testability Measures:
SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

UNIT -IV:
Built-In Self-Test:
The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per-Scan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST.

UNIT -V:
Boundary Scan Standard:
Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

TEXT BOOKS:
1. Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits – M.L. Bushnell, V. D. Agrawal, Kluwer Academic Pulishers.

REFERENCE BOOKS:
1. Digital Systems and Testable Design - M. Abramovici, M.A.Breuer and A.D Friedman, Jaico Publishing House. Digital Circuits Testing and Testability - P.K. Lala, Academic Press.

COURSE OUTCOMES:
After completing this course the students should be able to:
- Gain knowledge on digital testing as applied to VLSI design &Acquire knowledge on

testing of algorithms for digital circuits.

- Learn various testing methods for digital circuits & process of modern VLSI design, verification, and test.
- Develop and understanding for the advanced design concepts in modern VLSI technologies & Learn self-checking circuits where faults are detected by subcircuit called checker
- Gain the knowledge of testing and verification in VLSI design process, ATPG concepts for combinational and sequential circuits
- Specific techniques for designing high-speed, low-power, and easily-testable circuits

***

VAAGDEVI COLLEGE OF ENGINEERING
(AUTONOMOUS)

(M18VL13)LOW POWER VLSI DESIGN
(Program Elective – III)

M. Tech:II-Semester **L T P C**
3 0 0 3

COURSE OBJECTIVES:
- To design Low power CMOS designs, for digital circuits.
- To gain knowledge on low power circuit design styles for VLSI circuits.
- To understand power estimation and optimization methods for VLSI circuits.

UNIT –I:
Fundamentals:
Need for Low Power Circuit Design, Sources of Power Dissipation – Switching Power Dissipation,Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation, ShortChannel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

UNIT –II:
Low-Power Design Approaches:
Low-Power Design through Voltage Scaling – VTCMOS circuits, MTCMOS circuits, Architectural Level Approach –Pipelining and Parallel Processing Approaches.
Switched Capacitance Minimization Approaches:
System Level Measures, Circuit Level Measures, Mask level Measures.

UNIT –III:
Low-Voltage Low-Power Adders:
Introduction, Standard Adder Cells, CMOS Adder's Architectures – Ripple Carry Adders, Carry Look-Ahead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low-Power Design Techniques –Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles.

UNIT –IV:
Low-Voltage Low-Power Multipliers:
Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh- Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

UNIT –V:
Low-Voltage Low-Power Memories:
Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

TEXT BOOKS:
1. CMOS Digital Integrated Circuits – Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 2011.
2. Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering.

COURSE OUTCOMES:

After completing this course the students should be able to:

- Design Low power CMOS designs, for digital circuits & Gains knowledge on low power circuit design styles for VLSI circuits.
- Understand power estimation and optimization methods for VLSI circuits & causes of the power dissipation in digital ICs.
- Exploring the low power circuits and architectures for VLSI system.
- Understand the concept of VLSI circuit of low power operation & case study of low power design
- Design various circuits for optimize power

***

VAAGDEVI COLLEGE OF ENGINEERING
(AUTONOMOUS)

(M18VL14)OPTIMIZATION TECHNIQUES IN VLSI DESIGN
(Program Elective – III)

M. Tech:II-Semester **L T P C**
3 0 0 3

COURSE OBJECTIVES:
- To gain knowledge on Optimization techniques involved in VLSI circuits.
- To explore various Statistical modeling and performance analysis of VLSI Circuits..
- To understand the Concept of Genetic Algorithms and Routing Procedures.

UNIT –I:
Statistical Modeling:
Modeling sources of variations, Monte Carlo techniques, Process variation modeling- Pelgrom's model, Principle component based modeling, Quad tree based modeling, Performance modeling-Response surface methodology, delay modeling, interconnect delay models.

UNIT –II:
Statistical Performance, Power and Yield Analysis
Statistical timing analysis, parameter space techniques, Bayesian networks Leakage models, High level statistical analysis, Gate level statistical analysis, dynamic power, leakage power, temperature and power supply variations, High level yield estimation and gate level yield estimation.

UNIT –III:
Convex Optimization:
Convex sets, convex functions, geometric programming, trade-off and sensitivity analysis,
Generalized geometric programming, geometric programming applied to digital circuit gate sizing, Floor planning, wire sizing, Approximation and fitting- Monomial fitting, Maxmonomial fitting, Posynomial fitting.

UNIT –IV:
Genetic Algorithm:
Introduction, GA Technology-Steady State Algorithm-Fitness Scaling-Inversion GA for VLSI Design, Layout and Test automation- partitioning-automatic placement, routing technology, Mapping for FPGA- Automatic test generation- Partitioning algorithm Taxonomy-Multi-way Partitioning Hybrid genetic-encoding-local improvement-WDFR Comparison of CAS-Standard cell placement-GASP algorithm-unified algorithm.

UNIT –V:
GA Routing Procedures and Power Estimation:
Global routing-FPGA technology mapping-circuit generation-test generation in a GA frame work-test generation procedures, Power estimation-application of GA-Standard cell placement-GA for ATGproblem encoding- fitness function-GA Vs Conventional algorithm.

TEXT BOOKS / REFERENCE BOOKS:
1. Statistical Analysis and Optimization for VLSI: Timing and Power - Ashish Srivastava, Dennis Sylvester, David Blaauw, Springer, 2005.
2. Genetic Algorithm for VLSI Design, Layout and Test Automation - Pinaki Mazumder, E.Mrudnick, Prentice Hall,1998.
3. Convex Optimization – Stephen Boyd, Lieven Vandenberghe, Cambridge University

Press,

COURSE OUTCOMES:

After completing this course the students should be able to:

- Gain knowledge on Optimization techniques involved in VLSI circuits.
- Analyze methods of optimization to engineering students, including linear programming, nonlinear programming, and heuristic methods
- Understand balance between theory, numerical computation, problem setup for solution by optimization software, and applications to engineering systems.
- Studies General optimization algorithm; necessary and sufficient conditions for optimality
- Demonstrate the Concept of Genetic Algorithms and Routing Procedures

***

VAAGDEVI COLLEGE OF ENGINEERING
(AUTONOMOUS)

(M18VL15)HIGH SPEED VLSI DESIGN
(Program Elective – III)

M. Tech:II-Semester **L T P C**
3 0 0 3

COURSE OBJECTIVES:
- To gain knowledge on circuits and techniques involved in high speed VLSI circuits.
- To explore various design strategies to be followed for designing a high speed VLSI circuits.
- To understand the logic styles for designing a high speed VLSI circuit.

UNIT I - CLOCKED LOGIC STYLES:
Clocked Logic Styles, Single-Rail Domino Logic Styles, Dual-Rail Domino Structures, Latched Domino Structures, Clocked pass Gate Logic Non Clocked Logic Styles, Static CMOS, DCVS Logic, Non-Clocked pass Gate Families.

UNIT II - CIRCUIT DESIGN MARGINING AND DESIGN VARIABILITY:
Circuit Design Margining, Design Induced Variations, Process Induced Variations, Application Induced Variations, Noise.

UNIT III - LATCHING STRATEGIES:
Latching Strategies, Basic Latch Design, Latching Differential Logic, Race Free Latches for Pre-charged Logic, Asynchronous Latch Techniques.

UNIT IV - INTERFACE TECHNIQUES:
Signaling Standards, Chip-to-Chip Communication Networks, ESD Protection, Skew Tolerant Design

UNIT V - CLOCKING STYLES :
Clocking Styles, Clock Jitter, Clock Skew, Clock Generation, Clock Distribution, Asynchronous Clocking Techniques.

REFERENCES
1. Kerry Bernstein, Keith M. Carrig, “High Speed CMOS Design Styles”, Kluwer Academic Publishers, 2002.
2. Evan Sutherland, Bob Stroll, David Harris,” Logical Efforts, Designing Fast CMOS Circuits”, Kluwer Academic Publishers, 1999 3. David Harris, “Skew Tolerant Domino Design”, IEEE Journal of Solid State Circuits, 2001..

COURSE OUTCOMES:
After completing this course the students should be able to:
- Gain knowledge on circuits and techniques involved in high speed VLSI circuits.
- Explore various design strategies to be followed for designing a high speed VLSI circuits.
- Understand the logic styles for designing a high speed VLSI circuit & Learn the basics of VLSI design for high speed processing
- Apply methods for logical efforts, logic styles, latching strategies, interface techniques and related issues.
- Acquire knowledge about High Speed VLSI Circuits Design & Learn the basics of VLSI design for high speed processing

***

VAAGDEVI COLLEGE OF ENGINEERING
(AUTONOMOUS)

(M18VL16)ASIC DESIGN
(Program Elective – IV)

M. Tech:II-Semester

L	T	P	C
3	0	0	3

COURSE OBJECTIVES:

- To learn the fundamentals of ASIC and its design methods
- To gain knowledge on programmable architectures for ASICs
- To understand the physical design of ASIC.

UNIT I - INTRODUCTION TO ASIC'S

Types of ASICs - Design flow - CMOS transistors CMOS Design rules - Combinational Logic Cell - Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort - Library cell design - Library architecture .

UNIT II - PROGRAMMABLE ASIC'S

Anti fuse - static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT - Xilinx LCA -Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs – Xilinx I/O blocks.

UNIT III - PROGRAMMABLE ASIC LOGIC CELLS

Actel ACT -Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX 9000 - Altera FLEX -Design systems – Logic Synthesis – Half gate ASIC -Schematic entry - Low level design language - PLA tools -EDIF- CFI design representation.

UNIT IV - ASIC FLOOR PLANNING, PLACEMENT AND ROUTING

ASIC Construction: Physical Design- System Partitioning- FPGA Partitioning- Partitioning Methods. Floorplanning and Placement: Floorplanning- Placement- Physical Design Flow. Rou ting: Global Routing - Detailed Routing- Special Routing. Design checks

UNIT V - OPTIMIZATION ALGORITHMS

Planar subset problem(PSP) -single layer global routing single layer detailed routing wire length and bend minimization technique -over the cell(OTC) Routing-multichip modules(MCM)-Programmable logic arrays-Transistor chaining-Weinberger Arrays-Gate Matrix Layout-1D compaction-2D compaction

REFERENCES

1. M. J. S. Smith , "Application Specific Integrated Circuits", Addison - Wesley Longman Inc., 1997.
2. Farzad Nekoogar and Faranak Nekoogar , "From ASICs to SOCs: A Practical Approach", Prentice Hall PTR, 2003.

COURSE OUTCOMES:

After completing this course the students should be able to

- To learn the fundamentals of ASIC and its design methods
- To gain knowledge on programmable architectures for ASICs & physical design of ASIC
- To prepare the student to be an entry level industrial standard cell ASIC or FPGA designer
- To give the student an understanding of issues and tools related to ASIC/FPGA design.

- Prepare the student for implementation, including timing, performance and power optimization, verification and manufacturing test

***

VAAGDEVI COLLEGE OF ENGINEERING
(AUTONOMOUS)

(M18VL17)SYSTEM ON CHIP ARCHITECTURE
(Program Elective – IV)

M. Tech:II-Semester **L T P C**
3 0 0 3

COURSE OBJECTIVES:
- To learn System on chip fundamentals, their applications.
- To gain knowledge on SOC design.
- To learn the various computation models of SOCs.

UNIT –I:
Introduction to the System Approach:
System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

UNIT –II:
Processors:
Introduction , Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

UNIT –III:
Memory Design for SOC:
Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, Models of Simple Processor – memory interaction.

UNIT -IV:
Interconnect Customization and Configuration:
Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT –V:
Application Studies / Case Studies:
SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.

TEXT BOOKS:
1. Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk, Wiely IndiaPvt. Ltd.
2. ARM System on Chip Architecture – Steve Furber –2nd Ed., 2000, Addison Wesley Professional.

REFERENCE BOOKS:

1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer
2. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM.
3. System on Chip Verification – Methodologies and Techniques –Prakash Rashinkar, Peter Paterson and Leena Singh L, 2001, Kluwer Academic Publishers.

COURSE OUTCOMES:

After completing this course the students should be able to:

- To learn the fundamentals of ASIC and its design methods
- To gain knowledge on programmable architectures for ASICs & physical design of ASIC
- To prepare the student to be an entry level industrial standard cell ASIC or FPGA designer
- To give the student an understanding of issues and tools related to ASIC/FPGA design.
- Prepare the student for implementation, including timing, performance and power optimization, verification and manufacturing test

***

VAAGDEVI COLLEGE OF ENGINEERING
(AUTONOMOUS)

(M18VL18)SEMICONDUCTOR MEMORY DESIGN AND TESTING
(Program Elective – IV)

M. Tech:II-Semester **L T P C**
3 0 0 3

COURSE OBJECTIVES:
- To know the design of MOS memories and the various precautionary methods to be used in their design.
- To gain knowledge on various testing methods of semiconductor memories.
- To get an overview on reliability of semiconductors and their testing.

UNIT -I:
Random Access Memory Technologies:
SRAM – SRAM Cell structures, MOS SRAM Architecture, MOS SRAM cell and peripheral circuit operation, Bipolar SRAM technologies, SOI technology, Advanced SRAM architectures and technologies, Application specific SRAMs, DRAM – DRAM technology development, CMOS DRAM, DRAM cell theory and advanced cell structures, BICMOS DRAM, soft error failure in DRAM, Advanced DRAM design and architecture, Application specific DRAM

UNIT -II:
Non-volatile Memories:
Masked ROMs, High density ROM, PROM, Bipolar ROM, CMOS PROMS, EPROM, Floating gate EPROM cell, One time programmable EPROM, EEPROM, EEPROM technology and architecture, Non-volatile SRAM, Flash Memories (EPROM or EEPROM), advanced Flash memory architecture

UNIT -III:
Memory Fault Modeling Testing and Memory Design for Testability and Fault Tolerance:
RAM fault modeling, Electrical testing, Pseudo Random testing, Megabit DRAM Testing, non-volatile memory modeling and testing, IDDQ fault modeling and testing, Application specific memory testing, RAM fault modeling, BIST techniques for memory

UNIT -IV:
Semiconductor Memory Reliability and Radiation Effects:
General reliability issues RAM failure modes and mechanism, Non-volatile memory reliability, reliability modeling and failure rate prediction, Design for Reliability, Reliability Test Structures, Reliability Screening and qualification, Radiation effects, Single Event Phenomenon (SEP), Radiation Hardening techniques, Radiation Hardening Process and Design Issues, Radiation Hardened Memory characteristics, Radiation Hardness Assurance and Testing, Radiation Dosimetry, Water Level Radiation Testing and Test structures

UNIT -V:
Advanced Memory Technologies and High-density Memory Packing Technologies: Ferroelectric RAMs (FRAMs), GaAs FRAMs, Analog memories, magneto resistive RAMs (MRAMs), Experimental memory devices, Memory Hybrids and MCMs (2D), Memory Stacks and MCMs (3D), Memory MCM testing and reliability issues, Memory cards, High Density Memory Packaging Future Directions

TEXT BOOKS:
1. Semiconductor Memories Technology – Ashok K. Sharma, 2002, Wiley.
2. Advanced Semiconductor Memories – Architecture, Design and Applications - Ashok K. Sharma- 2002, Wiley.

3. Modern Semiconductor Devices for Integrated Circuits – Chenming C Hu, 1st Ed., Prentice

COURSE OUTCOMES:

After completing this course the students should be able to:

- Know the design of MOS memories and the various precautionary methods to be used in their design
- Learn overview of memory chip design, DRAM circuits, voltage generators, performance analysis and design issues of ultra-low voltage memory circuits
- Acquire knowledge about High-Performance Subsystem Memories & Analyse RAM and DRAM Design
- Demonstrate Advanced Memory Technologies and High-density Memory Packing Technologies & Gains knowledge on various testing methods of semiconductor memories
- Get an overview on reliability of semiconductors and their testing

***

VAAGDEVI COLLEGE OF ENGINEERING
(AUTONOMOUS)

(M18AC02) STRESS MANAGEMENT

M. Tech:II-Semester **L T P C**
2 0 0 0

Course Objectives:

- This course provides understanding stress such as work related stress and individual stress
- This course serves time management such as importance of planning the day and developing concentration
- This course serves career plateau such as Identifying Career plateaus and Structural and Content Plateauing and Making a fresh start
- This course provides controlling crisis management
- This course provides self development

UNDERSTANDING STRESS

Meaning – Symptoms – Work Related Stress – Individual Stress – Reducing Stress -sources of stress –consequence of stress-burnout-symptoms of Burnout- stress verses Burnout-model of stress-strategies for coping stress (individual and organizational strategies) –case study

TIME MANAGEMENT

Techniques – Importance of Planning the day –developing concentration – Prioritizing Beginning at the start – Techniques for conquering procrastination – Sensible delegation – Taking the right breaks – Learning to say "No"

CAREER PLATEAU

Career plateau – Identifying Career plateaus – Structural and Content - Plateauing – Making a fresh start – Importance of Sabbaticals – Counseling out – Executive leasing – Sustaining a marketable Career.

CRISIS MANAGEMENT

Implications – People issues – Structure issues – Environmental issues – Learning to keep calm - Preventing interruptions – Controlling crisis – Pushing new ideas – Empowerment – Work place Humour, Developing a sense of Humour – Learning to laugh – role of group cohesion and team spirit.

SELF DEVELOPMENT

Improving personality – Leading with Integrity – Enhancing Creativity – Effective decision making – Sensible Communication – The Listening Game – Managing Self – Mediation for peace – Yoga for Life

TEXT BOOKS

1. Bhatia R.L., The Executive Track: An Action Plan for Self Development Wheeler Publishing, New Delhi
2. Charavathy.S.K, "Human Values for Manager", McGraw Hill/Henely Management Series

REFERENCES

1. Jeffr Davison, Managing Stress, Prentice Hall of India, New Delhi
2. Jerrold S Greenberg, Comprehensive Stress Management, Jain Books, 2009

COURSE OUTCOMES:

- Enhance of Physical strength and flexibility.
- Learn to relax and focus.
- Relieve physical and mental tension
- Improve work performance/ efficiency.

****

VAAGDEVI COLLEGE OF ENGINEERING
(AUTONOMOUS)

(M18VL19)ANALOG IC DESIGN LABORATORY

M. Tech:II-Semester **L T P C**
0 0 4 2

Note: Any 10 of the following digital/analog circuits are to be designed and implemented using Mentor Graphics / Tanner Tools/Microwind-DSCH/NG-Spice/Equivalent CAD tools.

COURSE OBJECTIVES:

- To design Various Characteristics of MOS Logic.
- To design Various Amplifier circuits using CMOS Logic.
- To design Various circuits using Different Logic Styles.
- To design Layout of Different logic circuits.

List of Experiments:

1. Design of DC Characteristics of MOS Transistor.
2. Design and simulation of MOS current sources and current mirrors.
3. Design and simulation of emitter follower circuit.
4. Design and simulation of differential amplifier.
5. Design and simulation of Clippers and Clampers
6. Design and simulation of any circuit using current source load.
7. Design and simulation of any circuit using current sink load.
8. Design and simulation of Common source Amplifier using any load.
9. Design and simulation of Common Drain Amplifier.
10. Post Layout Simulation of common source amplifier circuit.
11. Post Layout Simulation of current source/current mirror circuit.
12. Post Layout Simulation of differential Amplifier.

COURSE OUTCOMES:

After completing this course the students should be able to:

- -Design Various Characteristics of MOS Logic
- Design Various Amplifier circuits using CMOS Logic
- Design Various circuits using Different Logic Styles
- Design Layout of Different logic circuits

***

VAAGDEVI COLLEGE OF ENGINEERING
(AUTONOMOUS)

(M18VL20)MIXED SIGNAL VLSI LABORATORY

M. Tech:II-Semester **L T P C**
0 0 4 2

Note: Any 10 of the following digital/analog circuits are to be designed and implemented using Mentor Graphics / Tanner Tools/Microwind-DSCH/NG-Spice/Equivalent CAD tools.

COURSE OBJECTIVES:
- To design Various Amplifier circuits using CMOS Logic.
- To design Various Complex circuits using Different Logic Styles.
- To design Layout of Different logic circuits.

List of Experiments:

1. SPICE simulation of Cascode Amplifier.
2. SPICE simulation of Differential Amplifier using Switched capacitor.
3. SPICE simulation of Two stage Operational Amplifier.
4. SPICE simulation of Two stage Comparator Circuit
5. SPICE simulation of Inverting Amplifier.
6. SPICE simulation Sample and Hold Circuit.
7. SPICE simulation of PLL.
8. SPICE simulation of Latches/Flip flops using CMOS.
9. SPICE simulation of Combinational Circuit using Bi-CMOS Logic.
10. Post Layout Simulation of Combinational Circuit
11. Post Layout Simulation of Sequential Circuit.
12. Post Layout Simulation of Amplifier Circuit.

COURSE OUTCOMES:

After completing this course the students should be able to:

- Design Various Amplifier circuits using CMOS Logic
- Design Various Complex circuits using Different Logic Styles
- Design Layout of Different logic circuits
- Digital/analog circuits are to be designed and implemented using CAD tools.

***

VAAGDEVI COLLEGE OF ENGINEERING
(AUTONOMOUS)

(M18VL21) MINI PROJECT

M. Tech:II-Semester **L T P C**
0 0 4 2

COURSE OUTCOMES:

After the completion of this course, the students should be able to

- Use fundamental knowledge and skills in engineering and apply it effectively on a project.
- Understand the Product Development Process including budgeting through Mini Project.
- Plan for various activities of the mini project.
- Inculcate electronic hardware and software implementation skills .
- Manage any disputes and conflicts within and outside individually.
- Prepare a technical report based on the Mini project.
- Deliver technical seminar based on the Mini Project work carried out.

VAAGDEVI COLLEGE OF ENGINEERING
(AUTONOMOUS)

(M18VL22)HIGH SPEED VLSI ARCHITECTURES FOR DSP APPLICATIONS
(Program Elective- V)

M. Tech:III-Semester **L T P C**
3 0 0 3

COURSE OBJECTIVES:

- To know the various methods for implementation of DSP systems.
- To understand the various implementations of VLSI DSP architectures for Arithmetic operations
- To gain knowledge on low power DSP architectures.

UNIT I – UNFOLDING:

Algorithm for Unfolding- Properties of Unfolding- Critical Path- Unfolding and Retiming- Applications of Unfolding. Folding: Folding TransformationRegister Minimization Techniques- Lifetime analysis-Data Allocation using forward-Backward register Allocation- Register Minimization in Folded Architectures- Folding of Multirate Systems.

UNIT II - DIGITAL MULTIPLIER ARCHITECTURES:

Parallel Multipliers- Interleaved Floor-plan and Bit-Plane-Based Digital Filters- Bit-Serial Multipliers- Bit-serial Filter Design and ImplementationCanonic Signed Digit Arithmetic- Distributed Arithmetic.

UNIT III - REDUNDANT ARITHMETIC:

Redundant Number Representations- Carry-Free Radix-2 Addition and Subtraction- Hybrid Radix-4 Addition- Radix-2 Hybrid Redundant Multiplication Architectures- Data Format Conversion- Redundant to Non redundant Converter . Numerical Strength Reduction: Sub expression Elimination- Multiple Constant Multiplication- Sub expression sharing in Digital Filters- Additive and Multiplicative Number Splitting.

UNIT IV - SYNCHRONOUS AND ASYNCHRONOUS PIPELINING:

Synchronous Pipelining and Clocking Styles- Clock Skew and Clock Distribution in Bit-Level Pipelined VLSI Designs- Wave PipeliningConstraint Space Diagram and Degree of Wave Pipelining- Implementation of Wave-Pipelined Systems- Asynchronous Pipelining- Signal Transition Graphs- Use of STG to Design Interconnection Circuits- - Implementation of Computational Units.

UNIT V - LOW POWER VLSI DSP SYSTEMS:

Theoretical Background- Scaling Versus Power Consumption- Power Analysis- Power Reduction Techniques- Power Estimation Approaches.- Simulation Based Approach.

REFERENCES

1. K.K Parhi, “VLSI Digital Signal processing”, John-Wiley 2008.
2. Behrooz Parhami, “Computer Arithmetic : Algorithms & Hardware Designs”, Oxford

University Press, 2nd Edition, 2010.

COURSE OUTCOMES:

- After completing this course the students should be able to:
- Know about the graph representations of DSP algorithms, Convolution algorithms and the concept of parallel recursive and adaptive filters
- Analyze The graph representations of DSP algorithms, Convolution algorithms & concept of parallel recursive and adaptive filters
- Gain the idea of scaling and round off noise and about digital lattice filter structures
- Contribute the knowledge in the design of parallel recursive and adaptive filters
- Demonstrate variable description of digital filters and digital lattice filter structures

***

VAAGDEVI COLLEGE OF ENGINEERING
(AUTONOMOUS)

(M18VL23)NANO MATERIALS & NANO TECHNOLOGY
(Program Elective- V)

M. Tech:III-Semester **L T P C**
3 0 0 3

COURSE OBJECTIVES:
- To learn the various limitation on MOSFETS and the alternates.
- To gain knowledge on SET and Carbon nano tubes in the design of transistors
- To learn the basics of molecular electronics and spintronics.

UNIT I - LIMITATION OF MOSFETS:
Classical mechanics and its drawbacks, Quantum mechanics, 1D problem - particle in a box, electron tunneling., MOSFET scaling, Non-uniform doping in channel, high K dielectrics, SOI MOSFET, Buried channel MOSFET, Fin FET.

UNIT II - SINGLE ELECTRONICS:
Coulomb blockade, Electron tunnelling devices, Single electron transistors , Resonant Tunneling Diodes- principle and applications, Quantum computing, Quantum cellular automata

UNIT III- CARBON NANO TUBES:
Carbon nano tubes – Basic structures, CNTFETs, Applications.

UNIT IV - MOLECULAR ELECTRONICS:
Molecular wire conductance - Theories of Coherent Electron Transport in molecular junctions, Evaluation of the conductance for coherent transport, Incoherent transport and vibronic coupling, Molecular circuit elements, Circuits.

UNIT V – SPINTRONICS:
Spin Vs charge, AMR, GMR, TMR, Spin devices- Spin valves, Magnetic tunnel junctions, Applications – memories (MRAM, STRAM), Logic device, and microwave oscillators.

REFERENCES:

1. Rainer Waser, “Nano Electronics and Information Technology: Advanced Electronic Materials
and Novel Devices”, 2nd Edition, Wiley-VCH, 2012.
2. Chonles P.Poole Jr., Frank. J. Owens, “Introduction to Nano technology”, John Wiley and Sons,
2009.
3. T. Pradeep, “Nano: The essentials”, Tata McGraw Hill, 2007. 4. Mark A. Ratner, Danill Ratner,
“Nano Technology: A Gentle Introduction to the Next Big Idea”, Prentice Hall, 2003.

COURSE OUTCOMES:
After completing this course the students should be able to:
- Understand the fundamental function of cells, and how nanotechnologies interact & Describe the various applications of nanotechnology in biotechnology & medicine.with cells.
- Explain the process of self-assembly – from single molecules into nanoparticles

- Describe and explain how nanoparticles are fabricated and characterized & principles of loading small molecule drugs, proteins or nucleic acids (DNA/RNA) into nanoparticles
- Describe and explain the scientific basis and medical benefits for using nanotechnology for treating diseases
- Demonstrate how nanotechnology-based innovation can drive better medicine and a stronger economy

***

VAAGDEVI COLLEGE OF ENGINEERING
(AUTONOMOUS)

(M18VL24)RF CIRCUIT DESIGN
(Program Elective- V)

M. Tech:III-Semester **L T P C**
3 0 0 3

COURSE OBJECTIVES:
- To explore the various performance measures of RF circuits.
- To acquire knowledge on the design of RF filters, amplifiers and oscillators.

UNIT I -PERFORMANCE PARAMETERS OF RF CIRCUITS:
Gain Parameters, Non-linearity parameters, Noise figure, Phase Noise, Dynamic range, RF front end performance parameters, performance trade offs in an RF circuit.

UNIT II - FILTER DESIGN:
Modern filter design, Frequency and impedance scaling, High Pass filter design, Band pass filter design, Band reject filter design, the effects of finite Q.

UNIT III - HIGH FREQUENCY AMPLIFIER DESIGN:
Zeros as Bandwidth enhances, Shunt-series Amplifier, Bandwidth enhancement with frequency Doublers, Tuned amplifiers, Neutralization and unilateralization, cascaded Amplifiers, LNA Topologies.

UNIT IV - MIXERS AND OSCILLATORS:
Mixer fundamentals, Non linear systems as Linear mixers, multiplier based mixers, Subsampling mixers. Problems with purely linear oscillators, Tuned oscillator, Negative Resistance oscillators, frequency synthesis.

UNIT V - RF POWER AMPLIFIERS:
General considerations, Class A, AB, B & C Power amplifier, Class D, E & F amplifiers, modulation of power amplifiers, RF Power amplifier design examples.

REFERENCES:
1. Aleksandar Tasic, Wouter.A.Serdijn, John.R.Long, "Adaptive Low Power Circuits for Wireless Communication (Analog Circuits and Signal Processing)", Springer, 1st Edition, 2006.
2. Chris Bowick, "RF Circuit design", Newnes (An imprint of Elesvier Science), 1st Edition, 1997.
3. 3.Thomas.H. Lee, "The design of CMOS Radio-Frequency Integrated Circuits", Cambridge University Press, 2nd Edition, 2004.

COURSE OUTCOMES:
After completing this course the students should be able to:
- Understand the fundamental function of cells, and how nanotechnologies interact & Describe the various applications of nanotechnology in biotechnology & medicine.with cells.
- Explain the process of self-assembly – from single molecules into nanoparticles
- Describe and explain how nanoparticles are fabricated and characterized & principles of loading small molecule drugs, proteins or nucleic acids (DNA/RNA) into nanoparticles
- Describe and explain the scientific basis and medical benefits for using nanotechnology for treating diseases
    - Demonstrate how nanotechnology-based innovation can drive better medicine and a stronger economy

***

VAAGDEVI COLLEGE OF ENGINEERING
(AUTONOMOUS)

(M18CS12)SOFT COMPUTING TECHNIQUES
(Open Elective)

M. Tech:III-Semester **L T P C**
3 0 0 3

COURSE OBJECTIVES:
- To understand the concepts of soft computing techniques.
- To enable to develop applications of soft computing in real life problems.

UNIT – I: Fundamentals of Neural Networks & Feed Forward Networks

Basic Concept of Neural Networks, Human Brain, Models of an Artificial Neuron, Learning Methods, Neural Networks Architectures, Signal Layer Feed Forward Neural Network :The Perceptron Model, Multilayer Feed Forward Neural Network :Architecture of a Back Propagation Network(BPN), The Solution, Back propagation Learning, Selection of various Parameters in BPN. Application of Back propagation Networks in Pattern Recognition & Image Processing.

UNIT – II: Associative Memories & ART Neural Networks

Basic concepts of Linear Associator, Basic concepts of Dynamical systems, Mathematical Foundation of Discrete-Time Hop field Networks(HPF), Mathematical Foundation of Gradient-Type Hopfield Networks, Transient response of Continuous Time Networks, Applications of HPF in Solution of Optimization Problem: Minimization of the Traveling salesman tour length, Summing networks with digital outputs, Solving Simultaneous Linear Equations, Bidirectional Associative Memory Networks; Cluster Structure, Vector Quantization, Classical ART Networks, Simplified ART Architecture.

UNIT – III: Fuzzy Logic & Systems

Fuzzy sets, Crisp Relations, Fuzzy Relations, Crisp Logic, Predicate Logic, Fuzzy Logic, Fuzzy Rule based system, Defuzzification Methods, Applications: Greg Viot's Fuzzy Cruise Controller, Air Conditioner Controller.

UNIT – IV: Genetic Algorithms

Basic Concepts of Genetic Algorithms (GA), Biological background, Creation of Off springs, Working Principle, Encoding, Fitness Function, Reproduction, Inheritance Operators, Cross Over, Inversion and Deletion, Mutation Operator, Bit-wise Operators used in GA, Generational Cycle, Convergence of Genetic Algorithm.

UNIT – V: Hybrid Systems

Types of Hybrid Systems, Neural Networks, Fuzzy Logic, and Genetic Algorithms Hybrid, Genetic Algorithm based BPN: GA Based weight Determination, Fuzzy Back Propagation Networks: LR-type fuzzy numbers, Fuzzy Neuron, Fuzzy BP Architecture, Learning in Fuzzy BPN, Inference by fuzzy BPN.

TEXT BOOKS:

1. Introduction to Artificial Neural Systems – J.M.Zurada, Jaico Publishers
2. Neural Networks, Fuzzy Logic & Genetic Algorithms: Synthesis & Applications – S.Rajasekaran, G.A. Vijayalakshmi Pai, July 2011, PHI, New Delhi.
3. Genetic Algorithms by David E. Gold Berg, Pearson Education India, 2006.
4. Neural Networks & Fuzzy Sytems- Kosko.B., PHI, Delhi,1994.

REFERENCE BOOKS:

1. Artificial Neural Networks - Dr. B. Yagananarayana, 1999, PHI, New Delhi.
2. An introduction to Genetic Algorithms - Mitchell Melanie, MIT Press, 1998
3. Fuzzy Sets, Uncertainty and Information- Klir G.J. & Folger. T. A., PHI, Delhi, 1993.

COURSE OUTCOMES:

After completing this course the students should be able to:

- Understand important and unique engineering issues at microwave and millimeter wave frequency
- Learn microwave network theory and the use of scattering matrix
- Learn design criteria for waveguide and coaxial microwave components.
- Learn the application of these components in the design of useful systems such as radars, receivers, etc.
- Work in small teams and design, fabricate and test a useful microwave component or device, which may be designed using microstripline technology.

***

VAAGDEVI COLLEGE OF ENGINEERING
(AUTONOMOUS)

(M18MA02)GRAPH THEORY & OPTIMIZATION TECHNIQUES
(Open Elective)

M. Tech: III-Semester **L T P C**

4. **3 0 0 3**

COURSE OBJECTIVES:

- To impart a knowledge on basics of graph theory and its algorithms
- To impart a knowledge on basic optimization techniques.
- To impart a knowledge on various statistical methods in analyzing a sample.

UNIT –I BASICS OF GRAPH THEORY:
Graphs –data structures for graphs-sub graphs – operations on graph connectivity- networks and the maximum flow- minimum cut theorem- treesspanning trees- Rooted trees- matrix representation of graphs.

UNIT –II CLASSES OF GRAPH:
Eulerian graphs and Hamiltonian graphs - standard theorems- planar graphsEuler's formula – five color problem- coloring of graphs- chromatic number (vertex and edge) properties and examples- directed graphs

UNIT –III GRAPH ALGORITHMS:
Computer representation of graphs-Basic graph algorithms- minimal spanning tree algorithm - Kruskal and prim's algorithm- shortest path algorithms- Dijsktra's algorithm- DFS and BFS algorithms.

UNIT –IV OPTIMIZATION TECHNIQUES:
Linear programming- graphical methods- simplex method (Artificial variables not included) - transportation and assignment problems.

UNIT –V STATISTICS:
Tchebyshev's inequality – Maximum likelihood estimation- correlationpartial correlation- multiple correlations- regression- Multiple regressions.

REFERENCES:

1. S C Gupta, V K Kapoor," Fundamentals of Mathematical statistics", Sultan Chand & sons, 2002.
2. Narsngh Dev, "Graph theory with applications to engineering and computer science", Prentice Hall of IndiaLtd, 1998.
3. Hoffmann and Kunze," Linear algebra", PHI, 1994.
4. Rao S.S , " Engineering optimization : Theory and practice", New age International Pvt. Ltd, 3rd edition ,1998.

COURSE OUTCOMES:

After completing this course the students should be able to:

- Understand the concepts of probability & statics
- Identify the strength and weakness of different theories
- Design and employ appropriate method for solving computing problems
- Analyze and compare the methods.
- Solve computing problems independently.

***

VAAGDEVI COLLEGE OF ENGINEERING
(AUTONOMOUS)

(M18SE27) WASTE MANAGEMENT
(Open Elective)

M. Tech:III-Semester 1. **L T P C**
3 0 0 3

COURSE OBJECTIVES:
- To assess the activities involved for the proposed and determine the type, nature and estimated volumes of waste to be generated.
- To identify any potential environmental impacts from the generation of waste at the site.
- To recommend appropriate waste handling and disposal measures

Unit - I Introduction to Environment:
Ecosystem –meaning- Types -Components- Structure – Functions, Levels of organization in nature- Food chain and Trophic structure, Biogeochemical Cycles, Energy flow.

Unit - II Municipal solid waste:
Definition Sources and types of solid waste- composition and its determinants of Solid waste-factors influencing generation-quantity assessment of solid wastes-methods of sampling and characterization.

Unit - III Collection and Transfer Collection:
Collection of Solid waste – collection services – collection system, equipments – time and frequency of collection – labour requirement – factors affecting collection – analysis of collection system – collection routes – preparation of master schedules. Transfer and Transport: Need for transfer operation – transfer stations – types – transport means and methods – location of transport stations - Manpower requirement – collection routes: Transfer stations – selection of location, types & design requirements, operation & maintenance.

Unit – IV Processing Techniques and Recovery of Energy:
Processing techniques – purposes mechanical volume reduction – necessary equipments – chemical volume reduction – incinerators – mechanical size reduction selection of equipments – components separation – methods – drying and dewatering. 7 Recovery of Resources, conversion products and energy recovery – recoverable materials – processing and recovery systems – incineration with heat recovery.

Unit – V Disposal of Solid Wastes:
Refuse disposal – various methods – incinerations – principle features of an incinerator – site selection and plant layout of an incinerator - sanitary landfill- methods of operation – advantages and disadvantages of sanitary land fill - site selection – reactions accruing in completed landfills – gas and leachate movement and control – equipments necessary.

References:
1. George Techobanoglous et al,"Integrated Solid Waste Management" McGraw - Hill, 1993.
2. Techobanoglous Thiesen Ellasen; Solid Waste Engineering Principles and Management, McGraw - Hill 1997.
3. R.E.Landrefh and P.A.Rebers," Municipal Solid Wastes-Problems & Solutions" ,Lewis, 1997.
4. Manual on Municipal 1 Solid waste Management, CPHEEO, Ministry of Urban Development, Govt. Of. India, New Delhi, 2000. 5) Blide A.D.& Sundaresan, B.B,"Solid Waste Management in Developing Countries", INSDOC, 1993.

5. Ecology Science and Practice; Claude Fourie, Christian Ferra, Paul Medori, Tean Devaux, Oxford and IBH Publishing Co (Pvt) LTD, special Indian edition.

COURSE OUTCOMES:

- Understand how waste management practices protect environmental health and safety.
- Apply physical and chemical analysis on municipal solid wastes
- Enhance the route for solid waste collection and transport system.
- Develop a method to use energy from solid wastes
- Explain different methods of disposal of hazardous solid waste

VAAGDEVI COLLEGE OF ENGINEERING
(AUTONOMOUS)

(M18VL25)DISSERTATION PHASE - I

M. Tech:III-Semester 1. **L T P C**
0 0 20 10

COURSE OUTCOMES:

After the completion of this course, the students should be able to

- In Master's Project Phase-I, the students should select a recent topic from a reputed International Journal, preferably IEEE, ACM, Springer in the field that has direct or indirect relation to the area of specialization.
- After conducting a detailed literature survey, they should compare and analyze research work done and review recent developments in the area and prepare an initial design of the work to be carried out as Master's Project.
- It is mandatory that the students should refer National and International Journals and conference proceedings while selecting a topic for their Project.
- Emphasis should be given for introduction to the topic, literature survey, and scope of the proposed work along with some preliminary work carried out on the Project topic.

Students should submit a copy of Phase-I Project report covering the content discussed above and highlighting the features of work to be carried out in Phase-II of the Project.

****

VAAGDEVI COLLEGE OF ENGINEERING
(AUTONOMOUS)

(M18VL26)DISSERTATION PHASE - II

M. Tech:IV-Semester 1. **L T P C**
0 0 32 16

COURSE OUTCOMES:

After the completion of this course, the students should be able to

- Use Specialized knowledge and skills in engineering and apply it effectively on a project.
- Apply knowledge of the 'real world' situations that a professional engineer can encounter.
- Apply critical and creative thinking in the design of VLSI System Design projects.
- Demonstrate a sound technical knowledge of selected project topic.
- Demonstrate the skills and attitude of a professional engineer.
- Summarize an appropriate list of literature review, analyse previous work and relate them to current project.
- Deliver technical seminar based on the Project work carried out.
- Publish the conducted research work in a National / International Conference or Journal preferably IEEE, ACM, Springer and Scopus indexed/SC Indexed/ESCI.