ACADEMIC REGULATIONS
COURSE STRUCTURE
AND
DETAILED SYLLABUS

M.TECH
VLSI/ VLSI DESIGN/
VLSI SYSTEM DESIGN

(Applicable for the batches admitted from 2013-14)

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
KUKATPALLY, HYDERABAD – 500 085.

ACADEMIC REGULATIONS R13 FOR M. TECH. (REGULAR) DEGREE COURSE

Applicable for the students of M. Tech. (Regular) Course from the Academic Year 2013-14 and onwards

The M. Tech. Degree of Jawaharlal Nehru Technological University Hyderabad shall be conferred on candidates who are admitted to the program and who fulfil all the requirements for the award of the Degree.

1.0 ELIGIBILITY FOR ADMISSIONS

Admission to the above program shall be made subject to eligibility, qualification and specialization as prescribed by the University from time to time.

Admissions shall be made on the basis of merit/rank obtained by the candidates at the qualifying Entrance Test conducted by the University or on the basis of any other order of merit as approved by the University, subject to reservations as laid down by the Govt. from time to time.

2.0 AWARD OF M. TECH. DEGREE

2.1 A student shall be declared eligible for the award of the M. Tech. Degree, if he pursues a course of study in not less than two and not more than four academic years. However, he is permitted to write the examinations for two more years after four academic years of course work.

2.2 A student, who fails to fulfill all the academic requirements for the award of the degree within four academic years from the year of his admission, shall forfeit his seat in M. Tech. course.

2.3 The student shall register for all 88 credits and secure all the 88 credits.

2.4 The minimum instruction days in each semester are 90.

3.0 A. COURSES OF STUDY

The following specializations are offered at present for the M. Tech. course of study.

1. Advanced Manufacturing Systems
2. Aerospace Engineering/ Aeronautical Engineering
3. Automation
4. Biomedical Signal Processing and Instrumentation
5. Bio-Technology
6. CAD/CAM
7. Chemical Engineering
8. Communication Systems
9. Computer Networks
10. Computer Networks and Information Security
11. Computer Science
12. Computer Science and Engineering
13. Computers and Communication Engineering.
14. Construction Management
15. Control Engineering
16. Control Systems
17. Cyber Forensic / Cyber Security & Information Technology
18. Design for Manufacturing/ Design and Manufacturing
19. Digital Electronics and Communication Engineering.
20. Digital Electronics and Communication Systems
21. Digital Systems and Computer Electronics
22. Electrical Power Engineering
23. Electrical Power Systems
24. Electronics & Instrumentation

25. Electronics and Communication Engineering
26. Embedded Systems
27. Embedded Systems and VLSI Design
28. Energy Systems
29. Engineering Design
30. Environmental Engineering
31. Geoinformatics and Surveying Technology
32. Geotechnical Engineering.
33. Heating Ventilation & Air Conditioning.
34. Highway Engineering
35. Image Processing
36. Industrial Engineering and Management
37. Information Technology
38. Infrastructure Engineering
39. Machine Design
40. Mechatronics.
41. Microwave & Radar Engineering
42. Nano Technology
43. Neural Networks
44. Parallel Computing
45. Power and Industrial Drives
46. Power Electronics
47. Power Electronics and Electrical Drives
48. Power Engineering and Energy Systems
49. Power Plant Engineering & Energy Management
50. Power System Control and Automation
51. Power System with Emphasis H.V. Engineering / H.V. Engineering
52. Production Engineering.
53. Real Time Systems
54. Software Engineering
55. Structural Engineering
56. Systems & Signal Processing
57. Thermal Engineering.
58. Transportation Engineering
59. VLSI
60. VLSI and Embedded System/ Electronics Design Technology
61. VLSI Design
62. VLSI System Design
63. Web Technologies
64. Wireless and Mobile Communication

and any other course as approved by the University from time to time.

3.0 B. Departments offering M. Tech. Programmes with specializations are noted below:

Civil Engg.	Construction Management Environmental Engineering Geoinformatics and Surveying Technology Geotechnical Engineering Highway Engineering Infrastructure Engineering Structural Engineering Transportation Engineering
EEE	Control Engineering Control Systems Electrical Power Engineering Electrical Power Systems Power and Industrial Drives Power Electronics Power Electronics and Electrical Drives Power Engineering and Energy Systems Power Plant Engineering & Energy Management Power System Control and Automation Power System with Emphasis H.V. Engineering / H.V. Engineering
ME	Advanced Manufacturing Systems Automation CAD/CAM Design for Manufacturing/ Design and Manufacturing Energy Systems Engineering Design Heating Ventilation & Air Conditioning Industrial Engineering and Management Machine Design Mechatronics. Power Plant Engineering & Energy Management Production Engineering Thermal Engineering.
ECE	Biomedical Signal Processing and Instrumentation Communication Systems Computers and Communication Engineering. Digital Electronics and Communication Engineering. Digital Electronics and Communication Systems Digital Systems and Computer Electronics Electronics & Instrumentation Electronics and Communication Engineering Embedded Systems Embedded Systems and VLSI Design

	Microwave & Radar Engineering Systems & Signal Processing VLSI VLSI and Embedded System/ Electronics Design Technology VLSI Design VLSI System Design Wireless and Mobile Communication
CSE	Computer Networks Computer Networks and Information Security Computer Science Computer Science and Engineering Cyber Forensic / Cyber Security & Information Technology Image Processing Information Technology Neural Networks Parallel Computing Real Time Systems Software Engineering Web Technologies
Aeronautical Engg.	Aerospace Engineering / Aeronautical Engineering
Bio-technology	Bio-Technology
Chemical Engg.	Chemical Engineering
Nano Technology	Nano Technology

4.0 ATTENDANCE

The programs are offered on a unit basis with each subject being considered a unit.

4.1 A student shall be eligible to write University examinations if he acquires a minimum of 75% of attendance in aggregate of all the subjects.

4.2 Condonation of shortage of attendance in aggregate up to 10% (65% and above and below 75%) in each semester shall be granted by the College Academic Committee.

4.3 Shortage of Attendance below 65% in aggregate shall not be condoned.

4.4 Students whose shortage of attendance is not condoned in any semester are not eligible to write their end semester examination of that class and their registration shall stand cancelled.

4.5 A prescribed fee shall be payable towards condonation of shortage of attendance.

4.6 A student shall not be promoted to the next semester unless he satisfies the attendance requirement of the present semester, as applicable. They may seek readmission into that semester when offered next. If any candidate fulfills the attendance requirement in the present semester, he shall not be eligible for readmission into the same class.

4.7 A candidate shall put in a minimum required attendance at least in three (3) theory subjects in the present semester to get promoted to the next semester. In order to qualify for the award of the M. Tech. Degree, the candidate shall complete all the academic requirements of the subjects, as per the course structure.

4.8 A student shall not be promoted to the next semester unless he satisfies the attendance requirements of the previous semester including the days of attendance in sports, games, NCC and NSS activities.

5.0 EVALUATION

The performance of the candidate in each semester shall be evaluated subject-wise, with a maximum of 100 marks for theory and 100 marks for practicals, on the basis of Internal Evaluation and End Semester Examination.

5.1 For the theory subjects 60 marks shall be awarded based on the performance in the End Semester Examination and 40 marks shall be awarded based on the Internal Evaluation. The internal evaluation shall be made based on the average of the marks secured in the two Mid Term-Examinations conducted-one in the middle of the Semester and the other immediately after the completion of instruction. Each mid term examination shall be conducted for a total duration of 120 minutes with Part A as compulsory question (16 marks) which consists of four sub-questions and carries 4 marks each and Part B with 3 questions to be answered out of 5 questions each question for 8 marks. If any candidate is absent from any subject of a mid-term examination, an on-line test will be conducted for him by the University. The details of the Question Paper pattern for End Examination (Theory) is given below:

- The End semesters Examination will be conducted for 60 marks which consists of two parts viz. i).Part-A for 20 marks, ii). Part –B for 40 marks.
- Part-A is compulsory question where it consists of five questions one from each unit and carries four marks each. This will be treated as Question 1.
- Part-B consists of five Questions (numbered from 2 to 6) carries 8 marks each. Each of these questions is from one unit and may contain sub-questions. For each question there will be an “either” “or” choice (that means there will be two questions from each unit and the student should answer only one question)

5.2 For practical subjects, 60 marks shall be awarded based on the performance in the End Semester Examinations and 40 marks shall be awarded based on the day-to-day performance as Internal Marks.

5.3 There shall be two seminar presentations during I year I semester and II semester. For seminar, a student under the supervision of a faculty member, shall collect the literature on a topic and critically review the literature and submit it to the department in a report form and shall make an oral presentation before the Departmental Academic Committee consisting of Head of the Department, Supervisor and two other senior faculty members of the department. For each Seminar there will be only internal evaluation of 50 marks. A candidate has to secure a minimum of 50% of marks to be declared successful.

5.4 There shall be a Comprehensive Viva-Voce in II year I Semester. The Comprehensive Viva-Voce will be conducted by a Committee consisting of Head of the Department and two Senior Faculty members of the Department. The Comprehensive Viva-Voce is intended to assess the students’ understanding of various subjects he has studied during the M. Tech. course of study. The Comprehensive Viva-Voce is evaluated for 100 marks by the Committee. There are no internal marks for the Comprehensive Viva-Voce.

5.5 A candidate shall be deemed to have secured the minimum academic requirement in a subject if he secures a minimum of 40% of marks in the End semester Examination and a minimum aggregate of 50% of the total marks in the End Semester Examination and Internal Evaluation taken together.

5.6 In case the candidate does not secure the minimum academic requirement in any subject (as specified in 5.5) he has to reappear for the End semester Examination in that subject. A candidate shall be given one chance to re-register for each subject provided the internal marks secured by a candidate are less than 50% and so has failed in the end examination. In such a case, the candidate must re-register for the subject(s) and secure the required minimum attendance. The candidate’s attendance in the re-registered subject(s) shall be calculated separately to decide upon his eligibility for writing the end examination in those subject(s). In the event of the student taking another chance, his internal marks and end examination marks obtained in the previous attempt stand cancelled.

5.7 In case the candidate secures less than the required attendance in any subject, he shall not be permitted to write the End Examination in that subject. He shall re-register the subject when next offered.

5.8 Laboratory examination for M. Tech. courses must be conducted with two Examiners, one of them being the Laboratory Class Teacher and the second examiner shall be another Laboratory Teacher.

6.0 EVALUATION OF PROJECT/DISSERTATION WORK

Every candidate shall be required to submit a thesis or dissertation on a topic approved by the Project Review Committee.

6.1 A Project Review Committee (PRC) shall be constituted with Principal as Chairperson, Heads of all the Departments offering the M. Tech. programs and two other senior faculty members.

6.2 Registration of Project Work: A candidate is permitted to register for the project work after satisfying the attendance requirement of all the subjects, both theory and practical.

6.3 After satisfying 6.2, a candidate has to submit, in consultation with his project supervisor, the title, objective and plan of action of his project work to the Departmental Academic Committee for approval. Only after obtaining the approval of the Departmental Academic Committee can the student initiate the Project work.

6.4 If a candidate wishes to change his supervisor or topic of the project, he can do so with the approval of the Departmental Academic Committee. However, the Departmental Academic Committee shall examine whether or not the change of topic/supervisor leads to a major change of his initial plans of project proposal. If yes, his date of registration for the project work starts from the date of change of Supervisor or topic as the case may be.

6.5 A candidate shall submit his status report in a bound-form in two stages at least with a gap of 3 months between them.

6.6 The work on the project shall be initiated at the beginning of the II year and the duration of the project is two semesters. A candidate is permitted to submit Project Thesis only after successful completion of theory and practical course with the approval of PRC not earlier than 40 weeks from the date of registration of the project work. For the approval of PRC the candidate shall submit the draft copy of thesis to the Principal through Head of the Department and make an oral presentation before the PRC.

6.7 Three copies of the Project Thesis certified by the supervisor shall be submitted to the College/ School/Institute.

6.8 The thesis shall be adjudicated by one examiner selected by the University. For this, the Principal of the College shall submit a panel of 5 examiners, eminent in that field, with the help of the guide concerned and head of the department.

6.9 If the report of the examiner is not favourable, the candidate shall revise and resubmit the Thesis, in the time frame as decided by the PRC. If the report of the examiner is unfavourable again, the thesis shall be summarily rejected.

6.10 If the report of the examiner is favourable, Viva-Voce examination shall be conducted by a board consisting of the Supervisor, Head of the Department and the examiner who adjudicated the Thesis. The Board shall jointly report the candidate's work as one of the following:

A. Excellent

B. Good

C. Satisfactory

D. Unsatisfactory

The Head of the Department shall coordinate and make arrangements for the conduct of Viva- Voce examination.

If the report of the Viva-Voce is unsatisfactory, the candidate shall retake the Viva-Voce examination only after three months. If he fails to get a satisfactory report at the second Viva- Voce examination, he will not be eligible for the award of the degree.

7.0 AWARD OF DEGREE AND CLASS

After a student has satisfied the requirements prescribed for the completion of the program and is eligible for the award of M. Tech. Degree he shall be placed in one of the following four classes:

Class Awarded	% of marks to be secured
First Class with Distinction	70% and above
First Class	Below 70% but not less than 60%
Second Class	Below 60% but not less than 50%
Pass Class	Below 50% but not less than 40%

The marks in internal evaluation and end examination shall be shown separately in the memorandum of marks.

8.0 WITHHOLDING OF RESULTS

If the student has not paid the dues, if any, to the university or if any case of indiscipline is pending against him, the result of the student will be withheld and he will not be allowed into the next semester. His degree will be withheld in such cases.

9.0 TRANSITORY REGULATIONS

9.1 Discontinued, detained, or failed candidates are eligible for admission to two earlier or equivalent subjects at a time as and when offered.

9.2 The candidate who fails in any subject will be given two chances to pass the same subject; otherwise, he has to identify an equivalent subject as per R13 academic regulations.

10. GENERAL

10.1 Wherever the words “he”, “him”, “his”, occur in the regulations, they include “she”, “her”, “hers”.

10.2 The academic regulation should be read as a whole for the purpose of any interpretation.

10.3 In the case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Vice-Chancellor is final.

10.4 The University may change or amend the academic regulations or syllabi at any time and the changes or amendments made shall be applicable to all the students with effect from the dates notified by the University.

MALPRACTICES RULES

DISCIPLINARY ACTION FOR / IMPROPER CONDUCT IN EXAMINATIONS

	Nature of Malpractices/Improper conduct	Punishment
	If the candidate:	
1. (a)	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form of material concerned with or related to the subject of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the subject of the examination)	Expulsion from the examination hall and cancellation of the performance in that subject only.
(b)	Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that subject only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him.
2.	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject of the examination (theory or practical) in which the candidate is appearing.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that Semester/ year. The Hall Ticket of the candidate is to be cancelled and sent to the University.
3.	Impersonates any other candidate in connection with the examination.	The candidate who has impersonated shall be expelled from examination hall. The candidate is also debarred and forfeits the seat. The performance of the original candidate who has been impersonated, shall be cancelled in all the subjects of the examination (including practicals and project work) already appeared and shall not be allowed to appear for examinations of the remaining subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. If the imposter is an outsider, he will be handed over to the police and a case is registered against him.

4.	Smuggles in the Answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
5.	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.	Cancellation of the performance in that subject.
6.	Refuses to obey the orders of the Chief Superintendent/Assistant – Superintendent / any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the officer-in charge or any person on duty in or outside the examination hall of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the officer-in-charge, or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that subject and all other subjects the candidate(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. The candidates also are debarred and forfeit their seats. In case of outsiders, they will be handed over to the police and a police case is registered against them.
7.	Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.

8.	Possess any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat.
9.	If student of the college, who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to 8.	Student of the colleges expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat. Person(s) who do not belong to the College will be handed over to police and, a police case will be registered against them.
10.	Comes in a drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year.
11.	Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that subject and all other subjects the candidate has appeared including practical examinations and project work of that semester/year examinations.
12.	If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the University for further action to award suitable punishment.	

Malpractices identified by squad or special invigilators

1. Punishments to the candidates as per the above guidelines.
2. Punishment for institutions : (if the squad reports that the college is also involved in encouraging malpractices)
    (i) A show cause notice shall be issued to the college.
    (ii) Impose a suitable fine on the college.
    (iii) Shifting the examination centre from the college to another college for a specific period of not less than one year.

***

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.TECH - VLSI/ VLSI DESIGN/VLSI SYSTEM DESIGN

COURSE STRUCTURE AND SYLLABUS

I Year I Semester

Code	Group	Subject	L	P	Credits
		VLSI Technology and Design	3	-	3
		CMOS Analog Integrated Circuit Design	3	-	3
		CPLD and FPGA Architectures and Applications	3	-	3
		CMOS Digital Integrated Circuit Design	3	-	3
	Elective -I	Digital System Design Hardware Software Co-Design Device Modeling	3	-	3
	Elective -II	Advanced Operating Systems Micro Controllers for Embedded System Design Advanced Computer Architecture	3	-	3
	Lab	VLSI Laboratory – I	-	3	2
		Seminar	-	-	2
		Total Credits	18	3	22

I Year II Semester

Code	Group	Subject	L	P	Credits
		Low Power VLSI Design	3	-	3
		CAD for VLSI Circuits	3	-	3
		CMOS Mixed Signal Circuit Design	3	-	3
		Design for Testability	3	-	3
	Elective - III	Scripting Languages Digital Signal Processors and Architectures VLSI Signal Processing	3	-	3
	Elective – IV	Optimization Techniques in VLSI Design System On Chip Architecture Semiconductor Memory Design and Testing	3	-	3
	Lab	VLSI Laboratory – II	-	3	2
		Seminar	-	-	2
		Total Credits	18	3	22

II Year - I Semester

Code	Group	Subject	L	P	Credits
		Comprehensive Viva	-	-	2
		Project Seminar	0	3	2
		Project work	-	-	18
		Total Credits	-	3	22

II Year - II Semester

Code	Group	Subject	L	P	Credits
		Project work and Seminar	-	-	22
		Total Credits	-	-	22

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M. Tech – I Year – I Sem. (VLSI/VLSI Design/VLSI System Design)

VLSI TECHNOLOGY AND DESIGN

UNIT –I:

Review of Microelectronics and Introduction to MOS Technologies:

MOS, CMOS, BiCMOS Technology.

Basic Electrical Properties of MOS, CMOS & BiCMOS Circuits: $I_{ds} – V_{ds}$ relationships, Threshold Voltage V_T, G_m, G_{ds} and ω_o, Pass Transistor, MOS, CMOS & Bi CMOS Inverters, Z_{pu}/Z_{pd}, MOS Transistor circuit model, Latch-up in CMOS circuits.

UNIT –II:

Layout Design and Tools:

Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools.

Logic Gates & Layouts:

Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and Inductive interconnect delays.

UNIT –III:

Combinational Logic Networks:

Layouts, Simulation, Network delay, Interconnect design, Power optimization, Switch logic networks, Gate and Network testing.

UNIT –IV:

Sequential Systems:

Memory cells and Arrays, Clocking disciplines, Design, Power optimization, Design validation and testing.

UNIT –V:

Floor Planning:

Floor planning methods, Global Interconnect, Floor Plan Design, Off-chip connections.

TEXT BOOKS:

1. Essentials of VLSI Circuits and Systems, K. Eshraghian Eshraghian. D, A. Pucknell, 2005, PHI.
2. Modern VLSI Design – Wayne Wolf, 3rd Ed., 1997, Pearson Education.

REFERENCE BOOKS:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011.
2. Principals of CMOS VLSI Design – N.H.E Weste, K. Eshraghian, 2nd Ed., Addison Wesley.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M. Tech – I Year – I Sem. (VLSI/VLSI Design/VLSi System Design)

CMOS ANALOG INTEGRATED CIRCUIT DESIGN

UNIT -I:

MOS Devices and Modeling:

The MOS Transistor, Passive Components- Capacitor & Resistor, Integrated circuit Layout, CMOS Device Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

UNIT -II:

Analog CMOS Sub-Circuits:

MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

UNIT -III:

CMOS Amplifiers:

Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures.

UNIT -IV:

CMOS Operational Amplifiers:

Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power- Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of OP Amp.

UNIT -V:

Comparators:

Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

TEXT BOOKS:

1. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
2. Analysis and Design of Analog Integrated Circuits- Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer, Wiley India, Fifth Edition, 2010.

REFERENCE BOOKS:

1. Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edn, 2013.
2. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition.
3. CMOS: Circuit Design, Layout and Simulation- Baker, Li and Boyce, PHI.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M. Tech – I Year – I Sem. (VLSI/VLSI Design/VLSi System Design)

CPLD AND FPGA ARCHITECURES AND APPLICATIONS

UNIT-I:

Introduction to Programmable Logic Devices:

Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex Programmable Logic Devices – Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.

UNIT-II:

Field Programmable Gate Arrays:

Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications of FPGAs.

UNIT -III:

SRAM Programmable FPGAs:

Introduction, Programming Technology, Device Architecture, The Xilinx XC2000, XC3000 and XC4000 Architectures.

UNIT -IV:

Anti-Fuse Programmed FPGAs:

Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures.

UNIT -V:

Design Applications:

General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

TEXT BOOKS:

1. Field Programmable Gate Array Technology - Stephen M. Trimberger, Springer International Edition.
2. Digital Systems Design - Charles H. Roth Jr, Lizy Kurian John, Cengage Learning.

REFERENCE BOOKS:

1. Field Programmable Gate Arrays - John V. Oldfield, Richard C. Dorf, Wiley India.
2. Digital Design Using Field Programmable Gate Arrays - Pak K. Chan/Samiha Mourad, Pearson Low Price Edition.
3. Digital Systems Design with FPGAs and CPLDs - Ian Grout, Elsevier, Newnes.
4. FPGA based System Design - Wayne Wolf, Prentice Hall Modern Semiconductor Design Series.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M. Tech – I Year – I Sem. (VLSI/VLSI Design/VLSi System Design)

CMOS DIGITAL INTEGRATED CIRCUIT DESIGN

UNIT –I:

MOS Design:

Pseudo NMOS Logic – Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

UNIT –II:

Combinational MOS Logic Circuits:

MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, Complex Logic circuits design – Realizing Boolean expressions using NMOS gates and CMOS gates , AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

UNIT –III:

Sequential MOS Logic Circuits:

Behavior of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flipflop.

UNIT –IV:

Dynamic Logic Circuits:

Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

UNIT –V:

Semiconductor Memories:

Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory- NOR flash and NAND flash.

TEXT BOOKS:

1. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

REFERENCE BOOKS:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Digital Integrated Circuits – A Design Perspective, Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, 2nd Ed., PHI.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M. Tech – I Year – I Sem. (VLSI/VLSI Design/VLSi System Design)

DIGITAL SYSTEM DESIGN

(ELECTIVE -I)

UNIT -I:

Minimization and Transformation of Sequential Machines:

The Finite State Model – Capabilities and limitations of FSM – State equivalence and machine minimization – Simplification of incompletely specified machines.

Fundamental mode model – Flow table – State reduction – Minimal closed covers – Races, Cycles and Hazards.

UNIT -II:

Digital Design:

Digital Design Using ROMs, PALs and PLAs , BCD Adder, 32 – bit adder, State graphs for control circuits, Scoreboard and Controller, A shift and add multiplier, Array multiplier, Keypad Scanner, Binary divider.

UNIT -III:

SM Charts:

State machine charts, Derivation of SM Charts, Realization of SM Chart, Implementation of Binary Multiplier, dice game controller.

UNIT -IV:

Fault Modeling & Test Pattern Generation:

Logic Fault model – Fault detection & Redundancy- Fault equivalence and fault location –Fault dominance – Single stuck at fault model – Multiple stuck at fault models –Bridging fault model.

Fault diagnosis of combinational circuits by conventional methods – Path sensitization techniques, Boolean Difference method – Kohavi algorithm – Test algorithms – D algorithm, PODEM, Random testing, Transition count testing, Signature analysis and test bridging faults.

UNIT -V:

Fault Diagnosis in Sequential Circuits:

Circuit Test Approach, Transition Check Approach – State identification and fault detection experiment, Machine identification, Design of fault detection experiment

TEXT BOOKS:

1. Fundamentals of Logic Design – Charles H. Roth, 5th Ed., Cengage Learning.
2. Digital Systems Testing and Testable Design – Miron Abramovici, Melvin A. Breuer and Arthur D. Friedman- John Wiley & Sons Inc.
3. Logic Design Theory – N. N. Biswas, PHI.

REFERENCE BOOKS:

1. Switching and Finite Automata Theory – Z. Kohavi , 2nd Ed., 2001, TMH.
2. Digital Design – Morris Mano, M.D.Ciletti, 4th Edition, PHI.
3. Digital Circuits and Logic Design – Samuel C. Lee , PHI.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M. Tech – I Year – I Sem. (VLSI/VLSI Design/VLSi System Design)

HARDWARE - SOFTWARE CO-DESIGN

(ELECTIVE -I)

UNIT –I:

Co- Design Issues:

Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.

Co- Synthesis Algorithms:

Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

UNIT –II:

Prototyping and Emulation:

Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure

Target Architectures:

Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT –III:

Compilation Techniques and Tools for Embedded Processor Architectures:

Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT –IV:

Design Specification and Verification:

Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification

UNIT –V:

Languages for System – Level Specification and Design-I:

System – level specification, design representation for system level synthesis, system level specification languages.

Languages for System – Level Specification and Design-II:

Heterogeneous specifications and multi language co-simulation, the cosyma system and lycos system.

TEXT BOOKS:

1. Hardware / Software Co- Design Principles and Practice – Jorgen Staunstrup, Wayne Wolf – 2009, Springer.
2. Hardware / Software Co- Design - Giovanni De Micheli, Mariagiovanna Sami, 2002, Kluwer Academic Publishers.

REFERENCE BOOK:

1. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont - 2010 – Springer.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M. Tech – I Year – I Sem. (VLSI/VLSI Design/VLSI System Design)

DEVICE MODELING

(ELECTIVE -I)

UNIT -I:

Introduction to Semiconductor Physics:

Review of Quantum Mechanics, Boltzman transport equation, Continuity equation, Poisson equation.

Integrated Passive Devices:

Types and Structures of resistors and capacitors in monolithic technology, Dependence of model parameters on structures

UNIT -II:

Integrated Diodes:

Junction and Schottky diodes in monolithic technologies – Static and Dynamic behavior – Small and large signal models – SPICE models

Integrated Bipolar Transistor:

Types and structures in monolithic technologies – Basic model (Eber-Moll) – Gunmel - Poon model- dynamic model, Parasitic effects – SPICE model –Parameter extraction

UNIT -III:

Integrated MOS Transistor:

NMOS and PMOS transistor – Threshold voltage – Threshold voltage equations – MOS device equations – Basic DC equations second order effects – MOS models – small signal AC characteristics – MOS FET SPICE model level 1, 2, 3 and 4

UNIT -IV:

VLSI Fabrication Techniques: An overview of wafer fabrication, Wafer Processing – Oxidation – Patterning – Diffusion – Ion Implantation – Deposition – Silicon gate nMOS process – CMOS processes – n-well- p-well- twin tub- Silicon on insulator – CMOS process enhancements – Interconnects circuit elements

UNIT -V:

Modeling of Hetero Junction Devices: Band gap Engineering, Band gap Offset at abrupt Hetero Junction, Modified current continuity equations, Hetero Junction bipolar transistors (HBTs), SiGe

TEXT BOOKS:

1. Introduction to Semiconductor Materials and Devices – Tyagi M. S, 2008, John Wiley Student Edition.
2. Solid State Circuits – Ben G. Streetman, Prentice Hall, 1997

REFERENCE BOOKS:

1. Physics of Semiconductor Devices – Sze S. M, 2nd Edition, Mcgraw Hill, New York, 1981.
2. Introduction to Device Modeling and Circuit Simulation – Tor A. Fijedly, Wiley-Interscience, 1997.
3. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M. Tech – I Year – I Sem. (VLSI/VLSI Design/VLSI System Design)

ADVANCED OPERATING SYSTEMS

(ELECTIVE -II)

UNIT –I:

Introduction to Operating Systems:

Overview of computer system hardware, Instruction execution, I/O function, Interrupts, Memory hierarchy, I/O Communication techniques, Operating system objectives and functions, Evaluation of operating System

UNIT –II:

Introduction to UNIX and LINUX:

Basic Commands & Command Arguments, Standard Input, Output, Input / Output Redirection, Filters and Editors, Shells and Operations

UNIT –III:

System Calls:

System calls and related file structures, Input / Output, Process creation & termination.

Inter Process Communication:

Introduction, File and record locking, Client – Server example, Pipes, FIFOs, Streams & Messages, Name Spaces, Systems V IPC, Message queues, Semaphores, Shared Memory, Sockets & TLI.

UNIT –IV:

Introduction to Distributed Systems:

Goals of distributed system, Hardware and software concepts, Design issues.

Communication in Distributed Systems:

Layered protocols, ATM networks, Client - Server model, Remote procedure call and Group communication.

UNIT –V:

Synchronization in Distributed Systems:

Clock synchronization, Mutual exclusion, E-tech algorithms, Bully algorithm, Ring algorithm, Atomic transactions

Deadlocks:

Dead lock in distributed systems, Distributed dead lock prevention and distributed dead lock detection.

TEXT BOOKS:

1. The Design of the UNIX Operating Systems – Maurice J. Bach, 1986, PHI.
2. Distributed Operating System - Andrew. S. Tanenbaum, 1994, PHI.
3. The Complete Reference LINUX – Richard Peterson, 4th Ed., McGraw – Hill.

REFERENCE BOOKS:

1. Operating Systems: Internal and Design Principles - Stallings, 6th Ed., PE.
2. Modern Operating Systems - Andrew S Tanenbaum, 3rd Ed., PE.
3. Operating System Principles - Abraham Silberchatz, Peter B. Galvin, Greg Gagne, 7th Ed., John Wiley
4. UNIX User Guide – Ritchie & Yates.
5. UNIX Network Programming - W.Richard Stevens, 1998, PHI.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M. Tech – I Year – I Sem. (VLSI/VLSI Design/VLSI System Design)

MICROCONTROLLERS FOR EMBEDDED SYSTEM DESIGN

(ELECTIVE -II)

UNIT –I:

ARM Architecture:

ARM Design Philosophy, Registers, Program Status Register, Instruction Pipeline, Interrupts and Vector Table, Architecture Revision, ARM Processor Families.

UNIT –II:

ARM Programming Model – I:

Instruction Set: Data Processing Instructions, Addressing Modes, Branch, Load, Store Instructions, PSR Instructions, Conditional Instructions.

UNIT –III:

ARM Programming Model – II:

Thumb Instruction Set: Register Usage, Other Branch Instructions, Data Processing Instructions, Single-Register and Multi Register Load-Store Instructions, Stack, Software Interrupt Instructions

UNIT –IV:

ARM Programming:

Simple C Programs using Function Calls, Pointers, Structures, Integer and Floating Point Arithmetic, Assembly Code using Instruction Scheduling, Register Allocation, Conditional Execution and Loops.

UNIT –V:

Memory Management:

Cache Architecture, Polices, Flushing and Caches, MMU, Page Tables, Translation, Access Permissions, Context Switch.

TEXT BOOK:

1. ARM Systems Developer’s Guides- Designing & Optimizing System Software – Andrew N. Sloss, Dominic Symes, Chris Wright, 2008, Elsevier.

REFERENCE BOOK:

1. Embedded Microcomputer Systems, Real Time Interfacing – Jonathan W. Valvano – Brookes / Cole, 1999, Thomas Learning.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M. Tech – I Year – I Sem. (VLSI/VLSI Design/VLSI System Design)

ADVANCED COMPUTER ARCHITECTURE

(ELECTIVE -II)

UNIT -I:

Fundamentals of Computer Design:

Fundamentals of Computer design, Changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, measuring and reporting performance, Quantitative principles of computer design, Amdahl's law.

Instruction set principles and examples- Introduction, classifying instruction set- memory addressing- type and size of operands, Operations in the instruction set.

UNIT –II:

Pipelines:

Introduction, basic RISC instruction set, Simple implementation of RISC instruction set, Classic five stage pipe lined RISC processor, Basic performance issues in pipelining, Pipeline hazards, Reducing pipeline branch penalties.

Memory Hierarchy Design:

Introduction, review of ABC of cache, Cache performance, Reducing cache miss penalty, Virtual memory.

UNIT -III:

Instruction Level Parallelism (ILP) - The Hardware Approach:

Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo's approach, Branch prediction, High performance instruction delivery- Hardware based speculation.

ILP Software Approach:

Basic compiler level techniques, Static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues - Hardware verses Software.

UNIT –IV:

Multi Processors and Thread Level Parallelism:

Multi Processors and Thread level Parallelism- Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – Memory architecture, Synchronization.

UNIT –V:

Inter Connection and Networks:

Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters.

Intel Architecture: Intel IA-64 ILP in embedded and mobile markets Fallacies and pit falls.

TEXT BOOK:

1. John L. Hennessy, David A. Patterson - Computer Architecture: A Quantitative Approach, 3rd Edition, an Imprint of Elsevier.

REFERENCE BOOKS:

1. John P. Shen and Miikko H. Lipasti -, Modern Processor Design : Fundamentals of Super Scalar Processors
2. Computer Architecture and Parallel Processing - Kai Hwang, Faye A.Brigs., MC Graw Hill.
3. Advanced Computer Architecture - A Design Space Approach, Dezso Sima, Terence Fountain, Peter Kacsuk, Pearson Ed.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M. Tech – I Year – I Sem. (VLSI/VLSI Design/VLSI System Design)

VLSI LABORATORY – I

Note: All the following digital circuits are to be designed and implemented using Cadence / Mentor Graphics / Synopsys / Equivalent CAD tools.

VLSI Front End Design programs:

Programming can be done using any HDL complier, Verification of the Functionality of the module using functional Simulator, Timing Simulation for Critical Path time Calculation, Synthesis of module, Place & Route and implementation of design using FPGA/CPLD Devices.

1. HDL code to realize all the logic gates
2. Design and Simulation of Half and Full adders, Serial Binary Adder, Multi Precision Adder, Carry Look Ahead Adder.
3. Design of 2-to-4 decoder
4. Design of 8-to-3 encoder (without and with priority)
5. Design of 8-to-1 multiplexer and 1x8 Demultiplexer
6. Design of 4 bit binary to gray code converter
7. Design of 4-bit comparator
8. Design of flip flops: SR, D, JK, T
9. Design of 4-bit binary, BCD counters (synchronous/ asynchronous reset).
10. Design of a N- bit shift register of Serial- in Serial –out, Serial in parallel out, Parallel in Serial out and Parallel in Parallel Out.
11. Design of Sequence Detector (Finite State Machine- Mealy and Moore Machines).
12. Design of 4- Bit Multiplier and 4-bit Divider.
13. Design of ALU to Perform – ADD, SUB, AND, OR, 1’s compliment, 2’s Compliment, Multiplication and Division.
14. Design of Finite State Machine.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M. Tech – I Year – II Sem. (VLSI/VLSI Design/VLSI System Design)

LOW POWER VLSI DESIGN

UNIT –I:

Fundamentals:

Need for Low Power Circuit Design, Sources of Power Dissipation – Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation, Short Channel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

UNIT –II:

Low-Power Design Approaches:

Low-Power Design through Voltage Scaling – VTCMOS circuits, MTCMOS circuits, Architectural Level Approach –Pipelining and Parallel Processing Approaches.

Switched Capacitance Minimization Approaches:

System Level Measures, Circuit Level Measures, Mask level Measures.

UNIT –III:

Low-Voltage Low-Power Adders:

Introduction, Standard Adder Cells, CMOS Adder's Architectures – Ripple Carry Adders, Carry Look-Ahead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low-Power Design Techniques –Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles.

UNIT –IV:

Low-Voltage Low-Power Multipliers:

Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh-Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

UNIT –V:

Low-Voltage Low-Power Memories:

Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

TEXT BOOKS:

1. CMOS Digital Integrated Circuits – Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 2011.
2. Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering.

REFERENCE BOOKS:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Low Power CMOS Design – AnanthaChandrakasan, IEEE Press/Wiley International, 1998.
3. Low Power CMOS VLSI Circuit Design – Kaushik Roy, Sharat C. Prasad, John Wiley & Sons, 2000.
4. Practical Low Power Digital VLSI Design – Gary K. Yeap, Kluwer Academic Press, 2002.
5. Low Power CMOS VLSI Circuit Design – A. Bellamour, M. I. Elamasri, Kluwer Academic Press, 1995.
6. Leakage in Nanometer CMOS Technologies – Siva G. Narendran, AnathaChandrakasan, Springer, 2005.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M. Tech – I Year – II Sem. (VLSI/VLSI Design/VLSI System Design)

CAD FOR VLSI CIRCUITS

UNIT -I:

VLSI Physical Design Automation:

VLSI Design Cycle, New Trends in VLSI Design Cycle, Physical Design Cycle, New Trends in Physical Design Cycle, Design Styles, System Packaging Styles;

UNIT -II:

Partitioning, Floor Planning, Pin Assignment and Placement:

Partitioning – Problem formulation, Classification of Partitioning algorithms, Kernighan-Lin Algorithm, Simulated Annealing, Floor Planning – Problem formulation, Classification of floor planning algorithms, constraint based floor planning, Rectangular Dualization, Pin Assignment – Problem formulation, Classification of pin assignment algorithms, General and channel Pin assignments, Placement **–** Problem formulation, Classification of placement algorithms, Partitioning based placement algorithms;

UNIT -III:

Global Routing and Detailed Routing:

Global Routing – Problem formulation, Classification of global routing algorithms, Maze routing algorithms, Detailed Routing – Problem formulation, Classification of routing algorithms, Single layer routing algorithms;

UNIT -IV:

Physical Design Automation of FPGAs:

FPGA Technologies, Physical Design cycle for FPGAs, Partitioning, Routing – Routing Algorithm for the Non-Segmented model, Routing Algorithms for the Segmented Model;

Physical Design Automation of MCMs:

Introduction to MCM Technologies, MCM Physical Design Cycle.

UNIT -V:

Chip Input and Output Circuits:

ESD Protection, Input Circuits, Output Circuits and $L\left(\frac{di}{dt}\right)$ noise, On-chip clock Generation and Distribution, Latch-up and its prevention.

TEXT BOOKS:

1. Algorithms for VLSI Physical Design Automation by Naveed Shervani, 3rd Edition, 2005, Springer International Edition.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

REFERENCE BOOKS:

1. VLSI Physical Design Automation-Theory and Practice by Sadiq M Sait, Habib Youssef, World Scientific.
2. Algorithms for VLSI Design Automation, S. H. Gerez, 1999, Wiley student Edition, John Wiley and Sons (Asia) Pvt. Ltd.
3. VLSI Physical Design Automation by Sung Kyu Lim, Springer International Edition.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M. Tech – I Year – II Sem. (VLSI/VLSI Design/VLSI System Design)

CMOS MIXED SIGNAL CIRCUIT DESIGN

UNIT -I:

Switched Capacitor Circuits:

Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing, biquad filters.

UNIT -II:

Phased Lock Loop (PLL):

Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs-PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications

UNIT -III:

Data Converter Fundamentals:

DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters

UNIT -IV:

Nyquist Rate A/D Converters:

Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Time-interleaved converters.

UNIT -V:

Oversampling Converters:

Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multibit quantizers, Delta sigma D/A

TEXT BOOKS:

1. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition, 2002
2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
3. Analog Integrated Circuit Design- David A. Johns,Ken Martin, Wiley Student Edition, 2013

REFERENCE BOOKS:

1. CMOS Integrated Analog-to- Digital and Digital-to-Analog converters-Rudy Van De Plassche, Kluwer Academic Publishers, 2003
2. Understanding Delta-Sigma Data converters-Richard Schreier, Wiley Interscience, 2005.
3. CMOS Mixed-Signal Circuit Design - R. Jacob Baker, Wiley Interscience, 2009.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M. Tech – I Year – II Sem. (VLSI/VLSI Design/VLSI System Design)

DESIGN FOR TESTABILITY

UNIT -I:

Introduction to Testing:

Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

UNIT -II:

Logic and Fault Simulation:

Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation, ATPG.

UNIT -III:

Testability Measures:

SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

UNIT -IV:

Built-In Self-Test:

The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per-Scan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST.

UNIT -V:

Boundary Scan Standard:

Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

TEXT BOOK:

1. Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits - M.L. Bushnell, V. D. Agrawal, Kluwer Academic Pulishers.

REFERENCE BOOKS:

1. Digital Systems and Testable Design - M. Abramovici, M.A.Breuer and A.D Friedman, Jaico Publishing House.
2. Digital Circuits Testing and Testability - P.K. Lala, Academic Press.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M. Tech – I Year – II Sem. (VLSI/VLSI Design/VLSI System Design)

SCRIPTING LANGUAGES

(ELECTIVE -III)

UNIT -I:

Introduction to Scripts and Scripting:

Characteristics and uses of scripting languages, Introduction to PERL, Names and values, Variables and assignment, Scalar expressions, Control structures, Built-in functions, Collections of Data, Working with arrays, Lists and hashes, Simple input and output, Strings, Patterns and regular expressions, Subroutines, Scripts with arguments.

UNIT -II:

Advanced PERL:

Finer points of Looping, Subroutines, Using Pack and Unpack, Working with files, Navigating the file system, Type globs, Eval, References, Data structures, Packages, Libraries and modules, Objects, Objects and modules in action, Tied variables, Interfacing to the operating systems, Security issues.

UNIT -III:

TCL:

The TCL phenomena, Philosophy, Structure, Syntax, Parser, Variables and data in TCL, Control flow, Data structures, Simple input/output, Procedures, Working with Strings, Patterns, Files and Pipes, Example code.

UNIT -IV:

Advanced TCL:

The eval, source, exec and up-level commands, Libraries and packages, Namespaces, Trapping errors, Event-driven programs, Making applications 'Internet-aware', 'Nuts-and-bolts' internet programming, Security issues, running untrusted code, The C interface.

UNIT -V:

TK and JavaScript:

Visual tool kits, Fundamental concepts of TK, TK by example, Events and bindings, Geometry managers, PERL-TK.

JavaScript – Object models, Design Philosophy, Versions of JavaScript, The Java Script core language, Basic concepts of Pythan.

Object Oriented Programming Concepts (Qualitative Concepts Only): Objects, Classes, Encapsulation, Data Hierarchy.

TEXT BOOKS:

1. The World of Scripting Languages- David Barron, Wiley Student Edition, 2010.
2. Practical Programming in Tcl and Tk - Brent Welch, Ken Jones and Jeff Hobbs., Fourth edition.
3. Java the Complete Reference - Herbert Schildt, 7th Edition, TMH.

REFERENCE BOOKS:

1. Tcl/Tk: A Developer's Guide- Clif Flynt, 2003, Morgan Kaufmann Series.
2. Tcl and the Tk Toolkit- John Ousterhout, 2nd Edition, 2009, Kindel Edition.
3. Tcl 8.5 Network Programming book- Wojciech Kocjan and Piotr Beltowski, Packt Publishing.
4. Tcl/Tk 8.5 Programming Cookbook- Bert Wheeler.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M. Tech – I Year – II Sem. (VLSI/VLSI Design/VLSI System Design)

DIGITAL SIGNAL PROCESSORS AND ARCHITECTURES

(ELECTIVE -III)

UNIT –I:

Introduction to Digital Signal Processing:

Introduction, a Digital signal-processing system, the sampling process, discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation.

Computational Accuracy in DSP Implementations:

Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT –II:

Architectures for Programmable DSP Devices:

Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation UNIT, Programmability and Program Execution, Speed Issues, Features for External interfacing.

UNIT -III:

Programmable Digital Signal Processors:

Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX Instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX Processors, Pipeline Operation of TMS320C54XX Processors.

UNIT –IV:

Analog Devices Family of DSP Devices:

Analog Devices Family of DSP Devices – ALU and MAC block diagram, Shifter Instruction, Base Architecture of ADSP 2100, ADSP-2181 high performance Processor.

Introduction to Black fin Processor - The Black fin Processor, Introduction to Micro Signal Architecture, Overview of Hardware Processing Units and Register files, Address Arithmetic Unit, Control Unit, Bus Architecture and Memory, Basic Peripherals.

UNIT –V:

Interfacing Memory and I/O Peripherals to Programmable DSP Devices:

Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA).

TEXT BOOKS:

1. Digital Signal Processing – Avtar Singh and S. Srinivasan, Thomson Publications, 2004.
2. A Practical Approach To Digital Signal Processing - K Padmanabhan, R. Vijayarajeswaran, Ananthi. S, New Age International, 2006/2009.
3. Embedded Signal Processing with the Micro Signal Architecture: Woon-Seng Gan, Sen M. Kuo, Wiley-IEEE Press, 2007.

REFERENCE BOOKS:

1. Digital Signal Processors, Architecture, Programming and Applications – B. Venkataramani and M. Bhaskar, 2002, TMH.
2. Digital Signal Processing – Jonatham Stein, 2005, John Wiley.
3. DSP Processor Fundamentals, Architectures & Features – Lapsley et al. 2000, S. Chand & Co.
4. Digital Signal Processing Applications Using the ADSP-2100 Family by The Applications Engineering Staff of Analog Devices, DSP Division, Edited by Amy Mar, PHI.
5. The Scientist and Engineer's Guide to Digital Signal Processing by Steven W. Smith, Ph.D., California Technical Publishing, ISBN 0-9660176-3-3, 1997.
6. Embedded Media Processing by David J. Katz and Rick Gentile of Analog Devices, Newnes , ISBN 0750679123, 2005.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M. Tech – I Year – II Sem. (VLSI/VLSI Design/VLSI System Design)

VLSI SIGNAL PROCESSING

(ELECTIVE -III)

UNIT -I:

Introduction to DSP:

Typical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms.

Pipelining and Parallel Processing:

Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power.

Retiming:

Introduction – Definitions and Properties – Solving System of Inequalities – Retiming Techniques.

UNIT –II:

Folding and Unfolding:

Folding: Introduction -Folding Transform - Register minimization Techniques – Register minimization in folded architectures – folding of multirate systems.

Unfolding: Introduction – An Algorithm for Unfolding – Properties of Unfolding – critical Path, Unfolding and Retiming – Applications of Unfolding.

UNIT -III:

Systolic Architecture Design:

Introduction – Systolic Array Design Methodology – FIR Systolic Arrays – Selection of Scheduling Vector – Matrix Multiplication and 2D Systolic Array Design – Systolic Design for Space Representations contain Delays.

UNIT -IV:

Fast Convolution:

Introduction – Cook-Toom Algorithm – Winogard algorithm – Iterated Convolution – Cyclic Convolution – Design of Fast Convolution algorithm by Inspection.

UNIT -V:

Low Power Design:

Scaling Vs Power Consumption –Power Analysis, Power Reduction techniques – Power Estimation Approaches.

Programmable DSP: Evaluation of Programmable Digital Signal Processors, DSP Processors for Mobile and Wireless Communications, Processors for Multimedia Signal Processing.

TEXT BOOKS:

1. VLSI Digital Signal Processing- System Design and Implementation – Keshab K. Parhi, 1998, Wiley Inter Science.
2. VLSI and Modern Signal Processing – Kung S. Y, H. J. While House, T. Kailath, 1985, Prentice Hall.

REFERENCE BOOKS:

1. Design of Analog – Digital VLSI Circuits for Telecommunications and Signal Processing – Jose E. France, Yannis Tsividis, 1994, Prentice Hall.

2. VLSI Digital Signal Processing – Medisetti V. K, 1995, IEEE Press (NY), USA.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M. Tech – I Year – II Sem. (VLSI/VLSI Design/VLSI System Design)

OPTIMIZATION TECHNIQUES IN VLSI DESIGN

(ELECTIVE -IV)

UNIT –I:

Statistical Modeling:

Modeling sources of variations, Monte Carlo techniques, Process variation modeling- Pelgrom?s model, Principle component based modeling, Quad tree based modeling, Performance modeling-Response surface methodology, delay modeling, interconnect delay models.

UNIT –II:

Statistical Performance, Power and Yield Analysis

Statistical timing analysis, parameter space techniques, Bayesian networks Leakage models, High level statistical analysis, Gate level statistical analysis, dynamic power, leakage power, temperature and power supply variations, High level yield estimation and gate level yield estimation.

UNIT –III:

Convex Optimization:

Convex sets, convex functions, geometric programming, trade-off and sensitivity analysis, Generalized geometric programming, geometric programming applied to digital circuit gate sizing, Floor planning, wire sizing, Approximation and fitting- Monomial fitting, Maxmonomial fitting, Posynomial fitting.

UNIT –IV:

Genetic Algorithm:

Introduction, GA Technology-Steady State Algorithm-Fitness Scaling-Inversion GA for VLSI Design, Layout and Test automation- partitioning-automatic placement, routing technology, Mapping for FPGA- Automatic test generation- Partitioning algorithm Taxonomy-Multi-way Partitioning Hybrid genetic-encoding-local improvement-WDFR Comparison of CAS-Standard cell placement-GASP algorithm-unified algorithm.

UNIT –V:

GA Routing Procedures and Power Estimation:

Global routing-FPGA technology mapping-circuit generation-test generation in a GA frame work-test generation procedures, Power estimation-application of GA-Standard cell placement-GA for ATG-problem encoding-fitness function-GA Vs Conventional algorithm.

TEXT BOOKS / REFERENCE BOOKS:

1. Statistical Analysis and Optimization for VLSI: Timing and Power - Ashish Srivastava, Dennis Sylvester, David Blaauw, Springer, 2005.
2. Genetic Algorithm for VLSI Design, Layout and Test Automation - Pinaki Mazumder, E.Mrudnick, Prentice Hall,1998.
3. Convex Optimization - Stephen Boyd, Lieven Vandenberghe, Cambridge University Press, 2004.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M. Tech – I Year – II Sem. (VLSI/VLSI Design/VLSI System Design)

SYSTEM ON CHIP ARCHITECTURE

(ELECTIVE -IV)

UNIT –I:

Introduction to the System Approach:

System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

UNIT –II:

Processors:

Introduction , Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

UNIT –III:

Memory Design for SOC:

Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, Models of Simple Processor – memory interaction.

UNIT -IV:

Interconnect Customization and Configuration:

Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT –V:

Application Studies / Case Studies:

SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.

TEXT BOOKS:

1. Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk, Wiely India Pvt. Ltd.
2. ARM System on Chip Architecture – Steve Furber –2nd Ed., 2000, Addison Wesley Professional.

REFERENCE BOOKS:

1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer
2. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM.
3. System on Chip Verification – Methodologies and Techniques –Prakash Rashinkar, Peter Paterson and Leena Singh L, 2001, Kluwer Academic Publishers.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M. Tech – I Year – II Sem. (VLSI/VLSI Design/VLSI System Design)

SEMICONDUCTOR MEMORY DESIGN AND TESTING

(ELECTIVE -IV)

UNIT -I:

Random Access Memory Technologies:

SRAM – SRAM Cell structures, MOS SRAM Architecture, MOS SRAM cell and peripheral circuit operation, Bipolar SRAM technologies, SOI technology, Advanced SRAM architectures and technologies, Application specific SRAMs, DRAM – DRAM technology development, CMOS DRAM, DRAM cell theory and advanced cell structures, BICMOS DRAM, soft error failure in DRAM, Advanced DRAM design and architecture, Application specific DRAM

UNIT -II:

Non-volatile Memories:

Masked ROMs, High density ROM, PROM, Bipolar ROM, CMOS PROMS, EPROM, Floating gate EPROM cell, One time programmable EPROM, EEPROM, EEPROM technology and architecture, Non-volatile SRAM, Flash Memories (EPROM or EEPROM), advanced Flash memory architecture

UNIT -III:

Memory Fault Modeling Testing and Memory Design for Testability and Fault Tolerance: RAM fault modeling, Electrical testing, Pseudo Random testing, Megabit DRAM Testing, non-volatile memory modeling and testing, IDDQ fault modeling and testing, Application specific memory testing, RAM fault modeling, BIST techniques for memory

UNIT -IV:

Semiconductor Memory Reliability and Radiation Effects:

General reliability issues RAM failure modes and mechanism, Non-volatile memory reliability, reliability modeling and failure rate prediction, Design for Reliability, Reliability Test Structures, Reliability Screening and qualification, Radiation effects, Single Event Phenomenon (SEP), Radiation Hardening techniques, Radiation Hardening Process and Design Issues, Radiation Hardened Memory characteristics, Radiation Hardness Assurance and Testing, Radiation Dosimetry, Water Level Radiation Testing and Test structures

UNIT -V:

Advanced Memory Technologies and High-density Memory Packing Technologies: Ferroelectric RAMs (FRAMs), GaAs FRAMs, Analog memories, magneto resistive RAMs (MRAMs), Experimental memory devices, Memory Hybrids and MCMs (2D), Memory Stacks and MCMs (3D), Memory MCM testing and reliability issues, Memory cards, High Density Memory Packaging Future Directions

TEXT BOOKS:

1. Semiconductor Memories Technology – Ashok K. Sharma, 2002, Wiley.
2. Advanced Semiconductor Memories – Architecture, Design and Applications - Ashok K. Sharma-2002, Wiley.
3. Modern Semiconductor Devices for Integrated Circuits – Chenming C Hu, 1st Ed., Prentice Hall.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M. Tech – I Year – II Sem. (VLSI/VLSI Design/VLSI System Design)

VLSI LABORATORY - II

Note: All the following digital/analog circuits are to be designed and implemented using Cadence / Mentor Graphics / Synopsys / Equivalent CAD tools.

The design shall include Gate-level design/Transistor-level design/Hierarchical design/Verilog HDL or VHDL design, Logic synthesis, Simulation and verification, Scaling of CMOS Inverter for different technologies, study of secondary effects (temperature, power supply and process corners), Circuit optimization with respect to area, performance and/or power, Layout, Extraction of parasitics and back annotation, modifications in circuit parameters and layout consumption, DC/transient analysis, Verification of layouts (DRC, LVS).

VLSI Back End Design programs:

1. Introduction to layout design rules
2. Layout, physical verification, placement & route for complex design, static timing analysis, IR drop analysis and crosstalk analysis of the following:
    - CMOS inverter
    - CMOS NOR/ NAND gates
    - CMOS XOR and MUX gates
    - CMOS half adder and full adder
    - Static / Dynamic logic circuits (register cell)
    - Latch
    - Pass transistor
3. Layout of any combinational circuit (complex CMOS logic gate)- Learning about data paths
4. Introduction to SPICE simulation and coding of NMOS/CMOS circuit
5. SPICE simulation of basic analog circuits: Inverter / Differential amplifier
6. Analog Circuit simulation (AC analysis) – CS & CD amplifier
7. System level design using PLL