VAAGDEVI COLLEGE OF ENGINEERING
(Autonomous)
Billikunta, Warangal - 506 005, Telangana State (India)
M.Tech. (VLSI SYSTEM DESIGN)- R14 Regulations

COURSE STRUCTURE AND SYLLABUS

I Year - I Semester

Code	Group	Subject	L	P	Credits
		VLSI Technology and Design	3	0	3
		CMOS Analog Integrated Circuit Design	3	0	3
		CPLD and FPGA Architectures and Applications	3	0	3
		CMOS Digital Integrated Circuit Design	3	0	3
	Elective -I	Digital System Design	3	0	3
		Hardware Software Co-Design			
		Device Modeling			
	Elective -II	Advance Operating Systems	3	0	3
		Micro Controllers for Embedded System Design			
		Advanced Computer Architecture			
	Lab	VLSI Laboratory – I	0	3	2
		Seminar	-	-	2
		Total Credits	18	3	22

I Year - II Semester

Code	Group	Subject	L	P	Credits
		Low Power VLSI Design	3	0	3
		CAD for VLSI Circuits	3	0	3
		CMOS Mixed Signal Circuit Design	3	0	3
		Design for Testability	3	0	3
	Elective - III	Scripting Languages	3	0	3
		Digital Signal Processors and Architectures			
		VLSI Signal Processing			
	Elective – IV	Optimization Techniques in VLSI Design	3	0	3
		System On Chip Architecture			
		Semiconductor Memory Design and Testing			
	Lab	VLSI Laboratory – II	0	3	2
		Seminar	-	-	2
		Total Credits	18	3	22

II Year - I Semester

Code	Group	Subject	L	P	Credits
		Comprehensive Viva	-	-	2
		Project Seminar	0	3	2
		Project work	-	-	18
		Total Credits	-	3	22

II Year - II Semester

Code	Group	Subject	L	P	Credits
		Project work and Seminar	-	-	22
		Total Credits	-	-	22

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VLSI TECHNOLOGY AND DESIGN

UNIT –I:
Review of Microelectronics and Introduction to MOS Technologies:
MOS, CMOS, BiCMOS Technology.

Basic Electrical Properties of MOS, CMOS & BiCMOS Circuits: I_{ds} – V_{ds} relationships, Threshold Voltage V_T, G_m, G_{ds} and ω_o, Pass Transistor, MOS, CMOS & Bi CMOS Inverters, Z_{pu}/Z_{pd}, MOS Transistor circuit model, Latch-up in CMOS circuits.

UNIT –II:
Layout Design and Tools:
Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools.
Logic Gates & Layouts:
Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and Inductive interconnect delays.

UNIT –III:
Combinational Logic Networks:
Layouts, Simulation, Network delay, Interconnect design, Power optimization, Switch logic networks, Gate and Network testing.

UNIT –IV:
Sequential Systems:
Memory cells and Arrays, Clocking disciplines, Design, Power optimization, Design validation and testing.

UNIT –V:
Floor Planning:
Floor planning methods, Global Interconnect, Floor Plan Design, Off-chip connections.

TEXT BOOKS:

1. Essentials of VLSI Circuits and Systems, K. Eshraghian Eshraghian. D, A. Pucknell, 2005, PHI.
2. Modern VLSI Design – Wayne Wolf, 3rd Ed., 1997, Pearson Education.

REFERENCE BOOKS:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011.
2. Principals of CMOS VLSI Design – N.H.E Weste, K. Eshraghian, 2nd Ed., Addison Wesley.

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CMOS ANALOG INTEGRATED CIRCUIT DESIGN

UNIT -I:
MOS Devices and Modeling:
The MOS Transistor, Passive Components- Capacitor & Resistor, Integrated circuit Layout, CMOS Device Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

UNIT -II:
Analog CMOS Sub-Circuits:
MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

UNIT -III:
CMOS Amplifiers:
Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures.

UNIT -IV:
CMOS Operational Amplifiers:
Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power-Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of OP Amp.

UNIT -V:
Comparators:
Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

TEXT BOOKS:

1. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
2. Analysis and Design of Analog Integrated Circuits- Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer, Wiley India, Fifth Edition, 2010.

REFERENCE BOOKS:

1. Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edn, 2013.
2. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition.
3. CMOS: Circuit Design, Layout and Simulation- Baker, Li and Boyce, PHI.

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CPLD AND FPGA ARCHITECURES AND APPLICATIONS

UNIT-I:
Introduction to Programmable Logic Devices:
Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex Programmable Logic Devices – Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.

UNIT-II:
Field Programmable Gate Arrays:
Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications of FPGAs.

UNIT -III:
SRAM Programmable FPGAs:
Introduction, Programming Technology, Device Architecture, The Xilinx XC2000, XC3000 and XC4000 Architectures.

UNIT -IV:
Anti-Fuse Programmed FPGAs:
Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures.

UNIT -V:
Design Applications:
General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

TEXT BOOKS:

1. Field Programmable Gate Array Technology - Stephen M. Trimberger, Springer International Edition.
2. Digital Systems Design - Charles H. Roth Jr, Lizy Kurian John, Cengage Learning.

REFERENCE BOOKS:

1. Field Programmable Gate Arrays - John V. Oldfield, Richard C. Dorf, Wiley India.
2. Digital Design Using Field Programmable Gate Arrays - Pak K. Chan/Samiha Mourad, Pearson Low Price Edition.
3. Digital Systems Design with FPGAs and CPLDs - Ian Grout, Elsevier,Newnes.
4. FPGA based System Design - Wayne Wolf, Prentice Hall Modern Semiconductor Design Series.

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CMOS DIGITAL INTEGRATED CIRCUIT DESIGN

UNIT –I:
MOS Design:
Pseudo NMOS Logic – Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

UNIT –II:
Combinational MOS Logic Circuits:
MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, Complex Logic circuits design – Realizing Boolean expressions using NMOS gates and CMOS gates , AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

UNIT –III:
Sequential MOS Logic Circuits:
Behavior of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flipflop.

UNIT –IV:
Dynamic Logic Circuits:
Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

UNIT –V:
Semiconductor Memories:
Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory- NOR flash and NAND flash.

TEXT BOOKS:

1. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

REFERENCE BOOKS:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Digital Integrated Circuits – A Design Perspective, Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, 2nd Ed., PHI.

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DIGITAL SYSTEM DESIGN
(ELECTIVE -I)

UNIT -I:
Minimization and Transformation of Sequential Machines:
The Finite State Model – Capabilities and limitations of FSM – State equivalence and machine minimization – Simplification of incompletely specified machines.
Fundamental mode model – Flow table – State reduction – Minimal closed covers – Races, Cycles and Hazards.

UNIT -II:
Digital Design:
Digital Design Using ROMs, PALs and PLAs , BCD Adder, 32 – bit adder, State graphs for control circuits, Scoreboard and Controller, A shift and add multiplier, Array multiplier, Keypad Scanner, Binary divider.

UNIT -III:
SM Charts:
State machine charts, Derivation of SM Charts, Realization of SM Chart, Implementation of Binary Multiplier, dice game controller.

UNIT -IV:
Fault Modeling & Test Pattern Generation:
Logic Fault model – Fault detection & Redundancy- Fault equivalence and fault location –Fault dominance – Single stuck at fault model – Multiple stuck at fault models –Bridging fault model.
Fault diagnosis of combinational circuits by conventional methods – Path sensitization techniques, Boolean Difference method – Kohavi algorithm – Test algorithms – D algorithm, PODEM, Random testing, Transition count testing, Signature analysis and test bridging faults.

UNIT -V:
Fault Diagnosis in Sequential Circuits:
Circuit Test Approach, Transition Check Approach – State identification and fault detection experiment, Machine identification, Design of fault detection experiment

TEXT BOOKS:

1. Fundamentals of Logic Design – Charles H. Roth, 5th Ed., Cengage Learning.
2. Digital Systems Testing and Testable Design – Miron Abramovici, Melvin A. Breuer and Arthur D. Friedman- John Wiley & Sons Inc.
3. Logic Design Theory – N. N. Biswas, PHI

REFERENCE BOOKS:

1. Switching and Finite Automata Theory – Z. Kohavi , 2nd Ed., 2001, TMH
2. Digital Design – Morris Mano, M.D.Ciletti, 4th Edition, PHI.
3. Digital Circuits and Logic Design – Samuel C. Lee , PHI

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HARDWARE - SOFTWARE CO-DESIGN
(ELECTIVE -I)

UNIT –I:

Co- Design Issues:

Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.

Co- Synthesis Algorithms:

Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

UNIT –II:

Prototyping and Emulation:

Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure

Target Architectures:

Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT –III:

Compilation Techniques and Tools for Embedded Processor Architectures:

Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT –IV:

Design Specification and Verification:

Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification

UNIT –V:

Languages for System – Level Specification and Design-I:

System – level specification, design representation for system level synthesis, system level specification languages,

Languages for System – Level Specification and Design-II:

Heterogeneous specifications and multi language co-simulation, the cosyma system and lycos system.

TEXT BOOKS:

1. Hardware / Software Co- Design Principles and Practice – Jorgen Staunstrup, Wayne Wolf – 2009, Springer.
2. Hardware / Software Co- Design - Giovanni De Micheli, Mariagiovanna Sami, 2002, Kluwer Academic Publishers

REFERENCE BOOKS:

1. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont - 2010 – Springer

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DEVICE MODELLING
(ELECTIVE -I)

UNIT -I:
Introduction to Semiconductor Physics:
Review of Quantum Mechanics, Boltzman transport equation, Continuity equation, Poisson equation.
Integrated Passive Devices:
Types and Structures of resistors and capacitors in monolithic technology, Dependence of model parameters on structures

UNIT -II:
Integrated Diodes:
Junction and Schottky diodes in monolithic technologies – Static and Dynamic behavior – Small and large signal models – SPICE models
Integrated Bipolar Transistor:
Types and structures in monolithic technologies – Basic model (Eber-Moll) – Gunmel - Poon model-dynamic model, Parasitic effects – SPICE model –Parameter extraction

UNIT -III:
Integrated MOS Transistor:
NMOS and PMOS transistor – Threshold voltage – Threshold voltage equations – MOS device equations – Basic DC equations second order effects – MOS models – small signal AC characteristics – MOS FET SPICE model level 1, 2, 3 and 4

UNIT -IV:
VLSI Fabrication Techniques: An overview of wafer fabrication, Wafer Processing – Oxidation – Patterning – Diffusion – Ion Implantation – Deposition – Silicon gate nMOS process – CMOS processes – n-well- p-well- twin tub- Silicon on insulator – CMOS process enhancements – Interconnects circuit elements

UNIT -V:
Modeling of Hetero Junction Devices: Band gap Engineering, Band gap Offset at abrupt Hetero Junction, Modified current continuity equations, Hetero Junction bipolar transistors (HBTs), SiGe

TEXT BOOKS:

1. Introduction to Semiconductor Materials and Devices – Tyagi M. S, 2008, John Wiley Student Edition.
2. Solid State Circuits – Ben G. Streetman, Prentice Hall, 1997

REFERENCE BOOKS:

1. Physics of Semiconductor Devices – Sze S. M, 2nd Edition, Mcgraw Hill, New York, 1981.
2. Introduction to Device Modeling and Circuit Simulation – Tor A. Fijedly, Wiley-Interscience, 1997.
3. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011

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ADVANCED OPERATING SYSTEMS
(ELECTIVE -II)

UNIT –I:

Introduction to Operating Systems:

Overview of computer system hardware, Instruction execution, I/O function, Interrupts, Memory hierarchy, I/O Communication techniques, Operating system objectives and functions, Evaluation of operating System

UNIT –II:

Introduction to UNIX and LINUX:

Basic Commands & Command Arguments, Standard Input, Output, Input / Output Redirection, Filters and Editors, Shells and Operations

UNIT –III:

System Calls:

System calls and related file structures, Input / Output, Process creation & termination.

Inter Process Communication:

Introduction, File and record locking, Client – Server example, Pipes, FIFOs, Streams & Messages, Name Spaces, Systems V IPC, Message queues, Semaphores, Shared Memory, Sockets & TLI.

UNIT –IV:

Introduction to Distributed Systems:

Goals of distributed system, Hardware and software concepts, Design issues.

Communication in Distributed Systems:

Layered protocols, ATM networks, Client - Server model, Remote procedure call and Group communication.

UNIT –V:

Synchronization in Distributed Systems:

Clock synchronization, Mutual exclusion, E-tech algorithms, Bully algorithm, Ring algorithm, Atomic transactions

Deadlocks:

Dead lock in distributed systems, Distributed dead lock prevention and distributed dead lock detection.

TEXT BOOKS:

1. The Design of the UNIX Operating Systems – Maurice J. Bach, 1986, PHI.
2. Distributed Operating System - Andrew. S. Tanenbaum, 1994, PHI.
3. The Complete Reference LINUX – Richard Peterson, 4th Ed., McGraw –Hill.

REFERENCE BOOKS:

1. Operating Systems: Internal and Design Principles - Stallings, 6th Ed., PE.
2. Modern Operating Systems - Andrew S Tanenbaum, 3rd Ed., PE.
3. Operating System Principles - Abraham Silberchatz, Peter B. Galvin, Greg Gagne, 7th Ed., John Wiley
4. UNIX User Guide – Ritchie & Yates.
5. UNIX Network Programming - W.Richard Stevens, 1998, PHI.

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MICROCONTROLLERS FOR EMBEDDED SYSTEM DESIGN
(ELECTIVE -II)

UNIT –I:
ARM Architecture:
ARM Design Philosophy, Registers, Program Status Register, Instruction Pipeline, Interrupts and Vector Table, Architecture Revision, ARM Processor Families.

UNIT –II:
ARM Programming Model – I:
Instruction Set: Data Processing Instructions, Addressing Modes, Branch, Load, Store Instructions, PSR Instructions, Conditional Instructions.

UNIT –III:
ARM Programming Model – II:
Thumb Instruction Set: Register Usage, Other Branch Instructions, Data Processing Instructions, Single-Register and Multi Register Load-Store Instructions, Stack, Software Interrupt Instructions

UNIT –IV:
ARM Programming:
Simple C Programs using Function Calls, Pointers, Structures, Integer and Floating Point Arithmetic, Assembly Code using Instruction Scheduling, Register Allocation, Conditional Execution and Loops.

UNIT –V:
Memory Management:
Cache Architecture, Polices, Flushing and Caches, MMU, Page Tables, Translation, Access Permissions, Context Switch.

TEXT BOOKS:

1. ARM Systems Developer's Guides- Designing & Optimizing System Software – Andrew N. Sloss, Dominic Symes, Chris Wright, 2008, Elsevier.

REFERENCE BOOKS:

1. Embedded Microcomputer Systems, Real Time Interfacing – Jonathan W. Valvano – Brookes / Cole, 1999, Thomas Learning.

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ADVANCED COMPUTER ARCHITECTURE
(ELECTIVE -II)

UNIT -I:

Fundamentals of Computer Design:

Fundamentals of Computer design, Changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, measuring and reporting performance, Quantitative principles of computer design, Amdahl's law.

Instruction set principles and examples- Introduction, classifying instruction set- memory addressing-type and size of operands, Operations in the instruction set.

UNIT –II:

Pipelines:

Introduction, basic RISC instruction set, Simple implementation of RISC instruction set, Classic five stage pipe lined RISC processor, Basic performance issues in pipelining, Pipeline hazards, Reducing pipeline branch penalties.

Memory Hierarchy Design:

Introduction, review of ABC of cache, Cache performance, Reducing cache miss penalty, Virtual memory.

UNIT -III:

Instruction Level Parallelism (ILP) - The Hardware Approach:

Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo's approach, Branch prediction, High performance instruction delivery- Hardware based speculation.

ILP Software Approach:

Basic compiler level techniques, Static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues - Hardware verses Software.

UNIT –IV:

Multi Processors and Thread Level Parallelism:

Multi Processors and Thread level Parallelism- Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – Memory architecture, Synchronization.

UNIT –V:

Inter Connection and Networks:

Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters.

Intel Architecture: Intel IA-64 ILP in embedded and mobile markets Fallacies and pit falls.

TEXT BOOKS:

1. John L. Hennessy, David A. Patterson - Computer Architecture: A Quantitative Approach, 3rd Edition, an Imprint of Elsevier.

REFERENCE BOOKS:

1. John P. Shen and Miikko H. Lipasti -, Modern Processor Design : Fundamentals of Super Scalar Processors
2. Computer Architecture and Parallel Processing - Kai Hwang, Faye A.Brigs., MC Graw Hill.
3. Advanced Computer Architecture - A Design Space Approach, Dezso Sima, Terence Fountain, Peter Kacsuk, Pearson Ed.

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VLSI LABORATORY – I

Note: All the following digital circuits are to be designed and implemented using Cadence / Mentor Graphics / Synopsys / Equivalent CAD tools.

VLSI Front End Design programs:

Programming can be done using any HDL complier, Verification of the Functionality of the module using functional Simulator, Timing Simulation for Critical Path time Calculation, Synthesis of module, Place & Route and implementation of design using FPGA/CPLD Devices.

1. HDL code to realize all the logic gates
2. Design and Simulation of Half and Full adders, Serial Binary Adder, Multi Precision Adder, Carry Look Ahead Adder.
3. Design of 2-to-4 decoder
4. Design of 8-to-3 encoder (without and with priority)
5. Design of 8-to-1 multiplexer and 1x8 Demultiplexer
6. Design of 4 bit binary to gray code converter
7. Design of 4-bit comparator
8. Design of flip flops: SR, D, JK, T
9. Design of 4-bit binary, BCD counters (synchronous/ asynchronous reset).
10. Design of a N- bit shift register of Serial- in Serial –out, Serial in parallel out, Parallel in Serial out and Parallel in Parallel Out.
11. Design of Sequence Detector (Finite State Machine- Mealy and Moore Machines).
12. Design of 4- Bit Multiplier and 4-bit Divider.
13. Design of ALU to Perform – ADD, SUB, AND, OR, 1's compliment, 2's Compliment, Multiplication and Division.
14. Design of Finite State Machine.

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LOW POWER VLSI DESIGN

UNIT –I:

Fundamentals:

Need for Low Power Circuit Design, Sources of Power Dissipation – Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation, Short Channel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

UNIT –II:

Low-Power Design Approaches:

Low-Power Design through Voltage Scaling – VTCMOS circuits, MTCMOS circuits, Architectural Level Approach –Pipelining and Parallel Processing Approaches.

Switched Capacitance Minimization Approaches:

System Level Measures, Circuit Level Measures, Mask level Measures.

UNIT –III:

Low-Voltage Low-Power Adders:

Introduction, Standard Adder Cells, CMOS Adder's Architectures – Ripple Carry Adders, Carry Look-Ahead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low-Power Design Techniques –Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles.

UNIT –IV:

Low-Voltage Low-Power Multipliers:

Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh-Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

UNIT –V:

Low-Voltage Low-Power Memories:

Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

TEXT BOOKS:

1. CMOS Digital Integrated Circuits – Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 2011.
2. Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering.

REFERENCE BOOKS:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Low Power CMOS Design – AnanthaChandrakasan, IEEE Press/Wiley International, 1998.
3. Low Power CMOS VLSI Circuit Design – Kaushik Roy, Sharat C. Prasad, John Wiley & Sons, 2000.
4. Practical Low Power Digital VLSI Design – Gary K. Yeap, Kluwer Academic Press, 2002.
5. Low Power CMOS VLSI Circuit Design – A. Bellamour, M. I. Elamasri, Kluwer Academic Press, 1995.
6. Leakage in Nanometer CMOS Technologies – Siva G. Narendran, AnathaChandrakasan, Springer, 2005.

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CAD FOR VLSI CIRCUITS

UNIT -I:
VLSI Physical Design Automation:
VLSI Design Cycle, New Trends in VLSI Design Cycle, Physical Design Cycle, New Trends in Physical Design Cycle, Design Styles, System Packaging Styles;

UNIT -II:
Partitioning, Floor Planning, Pin Assignment and Placement:
Partitioning – Problem formulation, Classification of Partitioning algorithms, Kernighan-Lin Algorithm, Simulated Annealing, Floor Planning – Problem formulation, Classification of floor planning algorithms, constraint based floor planning, Rectangular Dualization, Pin Assignment – Problem formulation, Classification of pin assignment algorithms, General and channel Pin assignments, Placement **–** Problem formulation, Classification of placement algorithms, Partitioning based placement algorithms;

UNIT -III:
Global Routing and Detailed Routing:
Global Routing – Problem formulation, Classification of global routing algorithms, Maze routing algorithms, Detailed Routing – Problem formulation, Classification of routing algorithms, Single layer routing algorithms;

UNIT -IV:
Physical Design Automation of FPGAs:
FPGA Technologies, Physical Design cycle for FPGAs, Partitioning, Routing – Routing Algorithm for the Non-Segmented model, Routing Algorithms for the Segmented Model;
Physical Design Automation of MCMs:
Introduction to MCM Technologies, MCM Physical Design Cycle.

UNIT -V:
Chip Input and Output Circuits:

ESD Protection, Input Circuits, Output Circuits and $L\left(\frac{di}{dt}\right)$ noise, On-chip clock Generation and Distribution, Latch-up and its prevention.

TEXT BOOKS:

1. Algorithms for VLSI Physical Design Automation by Naveed Shervani, 3rd Edition, 2005, Springer International Edition.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

REFERENCE BOOKS:

1. VLSI Physical Design Automation-Theory and Practice by Sadiq M Sait, Habib Youssef, World Scientific.
2. Algorithms for VLSI Design Automation, S. H. Gerez, 1999, Wiley student Edition, John Wiley and Sons (Asia) Pvt. Ltd.
3. VLSI Physical Design Automation by Sung Kyu Lim, Springer International Edition.

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CMOS MIXED SIGNAL CIRCUIT DESIGN

UNIT -I:
Switched Capacitor Circuits:
Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing, biquad filters.

UNIT -II:
Phased Lock Loop (PLL):
Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs-PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications

UNIT -III:
Data Converter Fundamentals:
DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters

UNIT -IV:
Nyquist Rate A/D Converters:
Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Time-interleaved converters.

UNIT -V:
Oversampling Converters:
Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multibit quantizers, Delta sigma D/A

TEXT BOOKS:

1. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition, 2002
2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
3. Analog Integrated Circuit Design- David A. Johns,Ken Martin, Wiley Student Edition, 2013

REFERENCE BOOKS:

1. CMOS Integrated Analog-to- Digital and Digital-to-Analog converters-Rudy Van De Plassche, Kluwer Academic Publishers, 2003
2. Understanding Delta-Sigma Data converters-Richard Schreier, Wiley Interscience, 2005.
3. CMOS Mixed-Signal Circuit Design - R. Jacob Baker, Wiley Interscience, 2009.

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DESIGN FOR TESTABILITY

UNIT -I:
Introduction to Testing:
Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

UNIT -II:
Logic and Fault Simulation:
Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation, ATPG.

UNIT -III:
Testability Measures:
SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

UNIT -IV:
Built-In Self-Test:
The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per-Scan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST.

UNIT -V:
Boundary Scan Standard:
Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

TEXT BOOKS:

1. Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits - M.L. Bushnell, V. D. Agrawal, Kluwer Academic Pulishers.

REFERENCE BOOKS:

1. Digital Systems and Testable Design - M. Abramovici, M.A.Breuer and A.D Friedman, Jaico Publishing House.

Digital Circuits Testing and Testability - P.K. Lala, Academic Press.

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SCRIPTING LANGUAGES FOR VLSI
(ELECTIVE -III)

UNIT -I:

Introduction to Scripts and Scripting:

Characteristics and uses of scripting languages, Introduction to PERL, Names and values, Variables and assignment, Scalar expressions, Control structures, Built-in functions, Collections of Data, Working with arrays, Lists and hashes, Simple input and output, Strings, Patterns and regular expressions, Subroutines, Scripts with arguments.

UNIT -II:

Advanced PERL:

Finer points of Looping, Subroutines, Using Pack and Unpack, Working with files, Navigating the file system, Type globs, Eval, References, Data structures, Packages, Libraries and modules, Objects, Objects and modules in action, Tied variables, Interfacing to the operating systems, Security issues.

UNIT -III:

TCL:

The TCL phenomena, Philosophy, Structure, Syntax, Parser, Variables and data in TCL, Control flow, Data structures, Simple input/output, Procedures, Working with Strings, Patterns, Files and Pipes, Example code.

UNIT -IV:

Advanced TCL:

The eval, source, exec and up-level commands, Libraries and packages, Namespaces, Trapping errors, Event-driven programs, Making applications 'Internet-aware', 'Nuts-and-bolts' internet programming, Security issues, running untrusted code, The C interface.

UNIT -V:

TK and JavaScript:

Visual tool kits, Fundamental concepts of TK, TK by example, Events and bindings, Geometry managers, PERL-TK.

JavaScript – Object models, Design Philosophy, Versions of JavaScript, The Java Script core language, Basic concepts of Pythan.

Object Oriented Programming Concepts (Qualitative Concepts Only): Objects, Classes, Encapsulation, Data Hierarchy.

TEXT BOOKS:

1. The World of Scripting Languages- David Barron, Wiley Student Edition, 2010.
2. Practical Programming in Tcl and Tk - Brent Welch, Ken Jones and Jeff Hobbs., Fourth edition.
3. Java the Complete Reference - Herbert Schildt, 7th Edition, TMH.

REFERENCE BOOKS:

1. Tcl/Tk: A Developer's Guide- Clif Flynt, 2003, Morgan Kaufmann SerieS.
2. Tcl and the Tk Toolkit- John Ousterhout, 2nd Edition, 2009, Kindel Edition.
3. Tcl 8.5 Network Programming book- Wojciech Kocjan and Piotr Beltowski, Packt Publishing.
4. Tcl/Tk 8.5 Programming Cookbook- Bert Wheeler

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DIGITAL SIGNAL PROCESSORS AND ARCHITECTURES
(ELECTIVE -III)

UNIT –I:

Introduction to Digital Signal Processing:

Introduction, a Digital signal-processing system, the sampling process, discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation.

Computational Accuracy in DSP Implementations:

Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT –II:

Architectures for Programmable DSP Devices:

Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation UNIT, Programmability and Program Execution, Speed Issues, Features for External interfacing.

UNIT -III:

Programmable Digital Signal Processors:

Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX Instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX Processors, Pipeline Operation of TMS320C54XX Processors.

UNIT –IV:

Analog Devices Family of DSP Devices:

Analog Devices Family of DSP Devices – ALU and MAC block diagram, Shifter Instruction, Base Architecture of ADSP 2100, ADSP-2181 high performance Processor.

Introduction to Black fin Processor - The Black fin Processor, Introduction to Micro Signal Architecture, Overview of Hardware Processing Units and Register files, Address Arithmetic Unit, Control Unit, Bus Architecture and Memory, Basic Peripherals.

UNIT –V:

Interfacing Memory and I/O Peripherals to Programmable DSP Devices:

Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA).

TEXT BOOKS:

1. Digital Signal Processing – Avtar Singh and S. Srinivasan, Thomson Publications, 2004.
2. A Practical Approach To Digital Signal Processing - K Padmanabhan, R. Vijayarajeswaran, Ananthi. S, New Age International, 2006/2009
3. Embedded Signal Processing with the Micro Signal Architecture: Woon-Seng Gan, Sen M. Kuo, Wiley-IEEE Press, 2007

REFERENCE BOOKS:

1. Digital Signal Processors, Architecture, Programming and Applications – B. Venkataramani and M. Bhaskar, 2002, TMH.
2. Digital Signal Processing – Jonatham Stein, 2005, John Wiley.
3. DSP Processor Fundamentals, Architectures & Features – Lapsley et al. 2000, S. Chand & Co.
4. Digital Signal Processing Applications Using the ADSP-2100 Family by The Applications Engineering Staff of Analog Devices, DSP Division, Edited by Amy Mar, PHI
5. The Scientist and Engineer's Guide to Digital Signal Processing by Steven W. Smith, Ph.D., California Technical Publishing, ISBN 0-9660176-3-3, 1997
6. Embedded Media Processing by David J. Katz and Rick Gentile of Analog Devices, Newnes , ISBN 0750679123, 2005

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VLSI SIGNAL PROCESSING
(ELECTIVE -III)

UNIT -I:

Introduction to DSP:

Typical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms

Pipelining and Parallel Processing:

Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power

Retiming:

Introduction – Definitions and Properties – Solving System of Inequalities – Retiming Techniques

UNIT –II:

Folding and Unfolding:

Folding: Introduction -Folding Transform - Register minimization Techniques – Register minimization in folded architectures – folding of multirate systems

Unfolding: Introduction – An Algorithm for Unfolding – Properties of Unfolding – critical Path, Unfolding and Retiming – Applications of Unfolding

UNIT -III:

Systolic Architecture Design:

Introduction – Systolic Array Design Methodology – FIR Systolic Arrays – Selection of Scheduling Vector – Matrix Multiplication and 2D Systolic Array Design – Systolic Design for Space Representations contain Delays

UNIT -IV:

Fast Convolution:

Introduction – Cook-Toom Algorithm – Winograd algorithm – Iterated Convolution – Cyclic Convolution – Design of Fast Convolution algorithm by Inspection

UNIT -V:

Low Power Design:

Scaling Vs Power Consumption –Power Analysis, Power Reduction techniques – Power Estimation Approaches

Programmable DSP: Evaluation of Programmable Digital Signal Processors, DSP Processors for Mobile and Wireless Communications, Processors for Multimedia Signal Processing

TEXT BOOKS:

1. VLSI Digital Signal Processing- System Design and Implementation – Keshab K. Parhi, 1998, Wiley Inter Science.
2. VLSI and Modern Signal Processing – Kung S. Y, H. J. While House, T. Kailath, 1985, Prentice Hall.

REFERENCE BOOKS:

1. Design of Analog – Digital VLSI Circuits for Telecommunications and Signal Processing – Jose E. France, Yannis Tsividis, 1994, Prentice Hall.
2. VLSI Digital Signal Processing – Medisetti V. K, 1995, IEEE Press (NY), USA.

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OPTIMIZATION TECHNIQUES IN VLSI DESIGN
(ELECTIVE -IV)

UNIT –I:
Statistical Modeling:
Modeling sources of variations, Monte Carlo techniques, Process variation modeling- Pelgrom□s model, Principle component based modeling, Quad tree based modeling, Performance modeling-Response surface methodology, delay modeling, interconnect delay models.

UNIT –II:
Statistical Performance, Power and Yield Analysis
Statistical timing analysis, parameter space techniques, Bayesian networks Leakage models, High level statistical analysis, Gate level statistical analysis, dynamic power, leakage power, temperature and power supply variations, High level yield estimation and gate level yield estimation.

UNIT –III:
Convex Optimization:
Convex sets, convex functions, geometric programming, trade-off and sensitivity analysis, Generalized geometric programming, geometric programming applied to digital circuit gate sizing, Floor planning, wire sizing, Approximation and fitting- Monomial fitting, Maxmonomial fitting, Posynomial fitting.

UNIT –IV:
Genetic Algorithm:
Introduction, GA Technology-Steady State Algorithm-Fitness Scaling-Inversion GA for VLSI Design, Layout and Test automation- partitioning-automatic placement, routing technology, Mapping for FPGA- Automatic test generation- Partitioning algorithm Taxonomy-Multi-way Partitioning Hybrid genetic-encoding-local improvement-WDFR Comparison of CAS-Standard cell placement-GASP algorithm-unified algorithm.

UNIT –V:
GA Routing Procedures and Power Estimation:
Global routing-FPGA technology mapping-circuit generation-test generation in a GA frame work-test generation procedures, Power estimation-application of GA-Standard cell placement-GA for ATG-problem encoding- fitness function-GA Vs Conventional algorithm.

TEXT BOOKS / REFERENCE BOOKS:

1. Statistical Analysis and Optimization for VLSI: Timing and Power - Ashish Srivastava, Dennis Sylvester, David Blaauw, Springer, 2005.
2. Genetic Algorithm for VLSI Design, Layout and Test Automation - Pinaki Mazumder, E.Mrudnick, Prentice Hall,1998.
3. Convex Optimization - Stephen Boyd, Lieven Vandenberghe, Cambridge University Press, 2004.

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SYSTEM ON CHIP ARCHITECTURE
(ELECTIVE -IV)

UNIT –I:

Introduction to the System Approach:

System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

UNIT –II:

Processors:

Introduction , Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

UNIT –III:

Memory Design for SOC:

Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, Models of Simple Processor – memory interaction.

UNIT -IV:

Interconnect Customization and Configuration:

Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT –V:

Application Studies / Case Studies:

SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.

TEXT BOOKS:

1. Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk, Wiely India Pvt. Ltd.
2. ARM System on Chip Architecture – Steve Furber –2nd Ed., 2000, Addison Wesley Professional.

REFERENCE BOOKS:

1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer
2. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM.
3. System on Chip Verification – Methodologies and Techniques –Prakash Rashinkar, Peter Paterson and Leena Singh L, 2001, Kluwer Academic Publishers.

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SEMICONDUCTOR MEMORY DESIGN AND TESTING
(ELECTIVE -IV)

UNIT -I:

Random Access Memory Technologies:

SRAM – SRAM Cell structures, MOS SRAM Architecture, MOS SRAM cell and peripheral circuit operation, Bipolar SRAM technologies, SOI technology, Advanced SRAM architectures and technologies, Application specific SRAMs, DRAM – DRAM technology development, CMOS DRAM, DRAM cell theory and advanced cell structures, BICMOS DRAM, soft error failure in DRAM, Advanced DRAM design and architecture, Application specific DRAM

UNIT -II:

Non-volatile Memories:

Masked ROMs, High density ROM, PROM, Bipolar ROM, CMOS PROMS, EPROM, Floating gate EPROM cell, One time programmable EPROM, EEPROM, EEPROM technology and architecture, Non-volatile SRAM, Flash Memories (EPROM or EEPROM), advanced Flash memory architecture

UNIT -III:

Memory Fault Modeling Testing and Memory Design for Testability and Fault Tolerance: RAM fault modeling, Electrical testing, Pseudo Random testing, Megabit DRAM Testing, non-volatile memory modeling and testing, IDDQ fault modeling and testing, Application specific memory testing, RAM fault modeling, BIST techniques for memory

UNIT -IV:

Semiconductor Memory Reliability and Radiation Effects:

General reliability issues RAM failure modes and mechanism, Non-volatile memory reliability, reliability modeling and failure rate prediction, Design for Reliability, Reliability Test Structures, Reliability Screening and qualification, Radiation effects, Single Event Phenomenon (SEP), Radiation Hardening techniques, Radiation Hardening Process and Design Issues, Radiation Hardened Memory characteristics, Radiation Hardness Assurance and Testing, Radiation Dosimetry, Water Level Radiation Testing and Test structures

UNIT -V:

Advanced Memory Technologies and High-density Memory Packing Technologies: Ferroelectric RAMs (FRAMs), GaAs FRAMs, Analog memories, magneto resistive RAMs (MRAMs), Experimental memory devices, Memory Hybrids and MCMs (2D), Memory Stacks and MCMs (3D), Memory MCM testing and reliability issues, Memory cards, High Density Memory Packaging Future Directions

TEXT BOOKS:

1. Semiconductor Memories Technology – Ashok K. Sharma, 2002, Wiley.
2. Advanced Semiconductor Memories – Architecture, Design and Applications - Ashok K. Sharma- 2002, Wiley.
3. Modern Semiconductor Devices for Integrated Circuits – Chenming C Hu, 1st Ed., Prentice Hall.

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VLSI LABORATORY - II

Note: All the following digital/analog circuits are to be designed and implemented using Cadence / Mentor Graphics / Synopsys / Equivalent CAD tools.

The design shall include Gate-level design/Transistor-level design/Hierarchical design/Verilog HDL or VHDL design, Logic synthesis, Simulation and verification, Scaling of CMOS Inverter for different technologies, study of secondary effects (temperature, power supply and process corners), Circuit optimization with respect to area, performance and/or power, Layout, Extraction of parasitics and back annotation, modifications in circuit parameters and layout consumption, DC/transient analysis, Verification of layouts (DRC, LVS).

VLSI Back End Design programs:

1. Introduction to layout design rules
2. Layout, physical verification, placement & route for complex design, static timing analysis, IR drop analysis and crosstalk analysis of the following:
    - CMOS inverter
    - CMOS NOR/ NAND gates
    - CMOS XOR and MUX gates
    - CMOS half adder and full adder
    - Static / Dynamic logic circuits (register cell)
    - Latch
    - Pass transistor
3. Layout of any combinational circuit (complex CMOS logic gate)- Learning about datapaths
4. Introduction to SPICE simulation and coding of NMOS/CMOS circuit
5. SPICE simulation of basic analog circuits: Inverter / Differential amplifier
6. Analog Circuit simulation (AC analysis) – CS & CD amplifier
7. System level design using PLL