COURSE STRUCTURE
AND
DETAILED SYLLABUS

M.TECH
VLSI SYSTEM DESIGN

For
M.TECH TWO YEAR DEGREE PROGRAMME
(Applicable for the batches admitted from 2020-2021)

VAAGDEVI COLLEGE OF ENGINEERING
(Autonomous)
Bollikunta, Warangal-506 005
Telangana State, India.
M.Tech-VLSI System Design

VAAGDEVI COLLEGE OF ENGINEERING
(AUTONOMOUS)

ELECTRONICS & COMMUNICATION ENGINEERING
M.TECH VLSI SYSTEM DESIGN

COURSE STRUCTURE
(R20 Regulations applicable for the batches admitted from Academic Year 2020-21)

I SEMESTER

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Total Credits 16 00 08 18

II - SEMESTER

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Total Credits 14 00 12 18
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COURSE OBJECTIVES:

➢ To understand the fundamentals of IC technology.
➢ To understand the analysis and design of analog integrated circuits starting from basic building blocks to different implementations of the amplifiers in CMOS technology.

UNIT –I: MOS Design
Pseudo NMOS Logic – Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

UNIT –II: Combinational MOS Logic Circuits:
MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, Complex Logic circuits design – Realizing Boolean expressions using NMOS gates and CMOS gates, AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

UNIT –III: Sequential MOS Logic Circuits:
Behavior of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flipflop.

UNIT –IV: Dynamic Logic Circuits:
Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

UNIT –V: Semiconductor Memories:
Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory- NOR flash and NAND flash.

TEXT BOOKS:

REFERENCE BOOKS:

COURSE OUTCOMES:
After the completion of this course, the students should be able to
CO1: Define the basic of CMOS technology
CO2: Relate, compare, interpret and make the use of the best CMOS design techniques for implementation, analysis & design of Combinational& Sequential MOS logic circuits
CO3: Know & tell different types of memories and compare performance evaluation of each memory modules so they can be able to think & justify how to improve performance by taking different structures.
CO4: Define, simplify & justify which dynamic logic circuit can be used investigate CMOS circuits.
CO5: Recommend various CMOS techniques and also other device technologies based on circuit constraints requirement.

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M.Tech-VLSI System Design

VAAGDEVI COLLEGE OF ENGINEERING
(AUTONOMOUS)

(M20VL02) CMOS ANALOG INTEGRATED CIRCUIT DESIGN

M. TECH- I Semester

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COURSE OBJECTIVES:

- To understand the fundamentals of MOS devices & modeling
- To develop the ability to design & analyze MOS based Analog VLSI Circuits
- To develop the skills to design analog VLSI circuits for a given specification

UNIT –I: MOS Devices and Modeling


UNIT –II: Analog CMOS Sub-Circuits:

MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors- Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

UNIT –III: CMOS Amplifiers:

Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain, Amplifiers Architectures.

UNIT –IV: CMOS Operational Amplifiers:


UNIT –V: Comparators:

Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open- Loop-Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

TEXT BOOKS:


REFERENCE BOOKS:

2. CMOS: Circuit Design, Layout and Simulation-Baker, Li and Boyce, PHI.

COURSE OUTCOMES:

Upon completion of this course, students should demonstrate the ability to:

- **CO1**: Define the parameters of MOS Devices & can predict the performance or behaviour of Analog VLSI circuit.
- **CO2**: Analyze & characterize analog devices and systems to achieve performance specifications
- **CO3**: Understand the different topologies involved in the CMOS amplifier design
- **CO4**: Understand design issues & measurement techniques related to CMOS operational amplifier design
- **CO5**: Design & analyze the comparator for different topologies to achieve performance specifications

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COURSE OBJECTIVES:
- To understand the different abstract levels in Verilog for modeling digital circuits.
- The student will learn the basic CMOS circuit, characteristics and performance.
- The student will learn the designing of combinational and sequential circuits in CMOS.

UNIT I - BASIC CONCEPTS - VERILOG
Operators, Basic concepts, Identifiers, System task and functions, Value set, Data types, Parameters, Operands, Operators, Modules and ports, Gate-level Modeling, Dataflow Modeling, Behavioral Modeling, Switch level modeling, Tri state gates, MOS Switches, Bidirectional switches, User defined primitives, Combinational UDP, Sequential UDP. Introduction to synthesis, Verilog HDL synthesis-Synthesis Design flow Test bench.

UNIT II – BASICS OF MOS TRANSISTORS
MOS transistors- Threshold voltage - characteristics of MOS transistor channel length modulation - short channel effects - Design of Logic gates using NMOS, PMOS and CMOS, Stick diagrams- Transfer characteristics of CMOS inverter - Power dissipation – Delay and sizing of inverters.

UNIT III - CMOS – COMBINATIONAL CIRCUITS
Static CMOS design-complementary CMOS - static properties complementary CMOS design- Power consumption in CMOS logic gates dynamic or glitching transitions - Design techniques to reduce switching activity - Radioed logic-DC VSL - pass transistor logic - Differential pass transistor logic - Sizing of level restorer-Sizing in pass transistor-Dynamic CMOS design-Basic principles - Domino logic-optimization of Domino logic-NPCMOS-logic style selection - Designing logic for reduced supply voltages.

UNIT IV - CMOS – SEQUENTIAL CIRCUITS
Timing metrics for sequential circuit - latches Vs registers -static latches and registers - Bistability principle - multiplexer based latches-master slave edge triggered registers- non-ideal clock signals- low voltage static latches-static SR flip flop - Dynamic latches and registers- C2MOS register - Dual edge registers-True single phase clocked registers-pipelining to optimize sequential circuit latch Vs register based pipelines

UNIT V – SUB-SYSTEM DESIGN/ SYSTEM VERILOG

REFERENCES
COURSE OUTCOMES:
Upon completion of this course, students should demonstrate the ability to:

CO1: Understand the basic concepts of Verilog HDL, digital system design flow, timing, and synthesis and FPGA implementation issues.
CO2: Understand the basics of MOS transistors required for MOS based circuit & layout design
CO3: Know the different design technique for CMOS Combinational Circuit Design & able to select suitable design technique for given performance specification
CO4: Get an idea of the different design technique for CMOS Sequential Circuit Design & able to select suitable design technique for given performance specification
CO5: Understand the design flow from simulation to synthesizable / implementation level for VLSI based system design

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COURSE OBJECTIVES:

- To understand the fundamentals of DSP
- To learn various VLSI architectures for digital signal processing
- To enable the students to design VLSI system with high speed & low power
- To know the techniques of critical path & algorithmic strength reduction in the filter structures
- To encourage students to develop a working knowledge of the central ideas of implementation of DSP algorithm with optimized hardware

UNIT I - INTRODUCTION TO DIGITAL SIGNAL PROCESSING:
Linear System Theory- Convolution- Correlation - DFT- FFT- Basic concepts in FIR Filters and IIR Filters- Filter Realizations, Representation of DSP Algorithms-Block diagram-SFG-DFG.

UNIT II - ITERATION BOUND, PIPELINING AND PARALLEL PROCESSING OF FIR FILTER:

UNIT III - FAST CONVOLUTION AND ARITHMETIC STRENGTH REDUCTION IN FILTERS:
Cook-Toom Algorithm- Modified Cook-Toom Algorithm, Design of Fast Convolution Algorithm by Inspection, Winograd algorithm, Parallel FIR filters-Fast FIR algorithms-Two parallel and three parallel.

UNIT IV - PIPELINED AND PARALLEL RECURSIVE FILTERS:
Pipelining in 1st Order IIR Digital Filters- Pipelining in Higher- Order IIR Filters-Clustered Look ahead and Stable Clustered Look ahead- Parallel Processing for IIR Filters and Problems.


REFERENCES

COURSE OUTCOMES:
Upon completion of this course, students should demonstrate the ability to:
- CO1: Understand the overview of DSP concepts
- CO2: Apply the concepts of iteration bound, pipelining& parallel processing for FIR filter design
- CO3: Understand techniques of fast convolution & algorithmic strength reduction in the filter structures
- CO4: Perform pipelining & parallel processing on recursive filter structures to achieve high speed & low power
- CO5: Use of proper techniques for parallel processing design for scaling and round offnoise
VAAGDEVI COLLEGE OF ENGINEERING
(AUTONOMOUS)

(M20VL05)VLSI TECHNOLOGY
(Program Elective – I)

M. TECH- I Semester

COURSE OBJECTIVES:
- To understand the impact of the physical and chemical processes of integrated circuit fabrication technology on the design of integrated circuits.
- To understand physics of the Crystal growth, wafer fabrication and basic properties of silicon wafers.
- To learn the concepts of Design rules and Scaling, BICMOSICs.

UNIT –I:
Review of Microelectronics and Introduction to MOS Technologies:
MOS, CMOS, BiCMOS Technology. Basic Electrical Properties of MOS, CMOS & BiCMOS Circuits: Ids – Vds relationships, Threshold Voltage VT, Gm, Gdsand oo, Pass Transistor, MOS, CMOS & Bi CMOS Inverters, Zpu/Zpd, MOS Transistor circuit model, Latch-up in CMOS circuits.

UNIT –II:
Layout Design and Tools:

UNIT –III:
Overview of semiconductor industry, Stages of Manufacturing, Process and product trends, Crystal growth, Basic wafer fabrication operations, process yields, Semiconductor material preparation, Basic wafer fabrication operations, Yield measurement, Contamination sources, Clean room construction, Oxidation and Photolithography, Doping and Depositions, Metallization. Ten step patterning process, Photo resists, physical properties of photo resists, Storage and control of photo resists, photo masking process, Hard bake, develop inspect, Dry etching Wet etching, resist stripping

UNIT –IV
Doping and depositions: Diffusion process steps, deposition, Drive-in oxidation, Ion implantation-1, Ion implantation-2, CVD basics, CVD process steps, Low pressure CVD systems, Plasma enhanced CVD systems, Vapour phase epitaxy, molecular beam epitaxy.

UNIT –V
Design rules and Scaling, BICMOS ICs: Choice of transistor types, pnp transistors, Resistors, capacitors, Packaging: Chip characteristics, package functions, package operations

TEXT BOOKS:

REFERENCE BOOKS:
COURSE OUTCOMES:
Upon completion of this course, students should demonstrate the ability to:

CO1: Understand the different MOS technologies

CO2: Appreciate the various techniques involved in the VLSI fabrication process

CO3: Analyze the concepts, transistor structures, interconnects & design rules related to layout design in VLSI

CO4: Understand the different doping & diffusion mechanism

CO5: Understand the nuances of design rules, scaling, transistors, resistors, capacitors & packaging of VLSI devices

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M. TECH- I Semester

COURSE OBJECTIVES:

- Understand the concepts of Physical Design Process such as partitioning, Floor planning, Placement and Routing.
- Discuss the concepts of design optimization algorithms and their application to physical design automation.
- Understand the concepts of simulation and synthesis in VLSI Design Automation.
- Formulate CAD design problems using algorithmic methods.

UNIT I: PRELIMINARIES
Introduction to Design Methodologies, Design Automation tools, Algorithmic Graph Theory, Computational complexity, Tractable and Intractable problems.

UNIT II:
GENERAL PURPOSE METHODS FOR COMBINATIONAL OPTIMIZATION
Backtracking, Branch and Bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu search, Genetic Algorithms.

UNIT III:
LAYOUT COMPACTION, PLACEMENT, FLOORPLANNING AND ROUTING
Problems, Concepts and Algorithms.

MODELLING AND SIMULATION
Gate Level Modeling and Simulation, Switch level Modeling and Simulation.

UNIT IV:
LOGIC SYNTHESIS AND VERIFICATION
Basic issues and Terminology, Binary-Decision diagrams, Two-Level logic Synthesis

HIGH-LEVEL SYNTHESIS

UNIT V:
PHYSICAL DESIGN AUTOMATION OF FPGAs
FPGA technologies, Physical Design cycle for FPGAs, partitioning and Routing for segmented and staggered Models.

PHYSICAL DESIGN AUTOMATION OF MCMs
MCM technologies, MCM physical design cycle, Partitioning, Placement - Chip Array based and Full Custom Approaches, Routing – Maze routing, Multiple stage routing, Topologic routing, Integrated Pin Distribution and routing, Routing and Programmable MCMs.

TEXT BOOKS

REFERENCE BOOKS
COURSE OUTCOMES:
Upon completion of this course, students should demonstrate the ability to:

**CO1:** Understand the preliminaries required for VLSI system design

**CO2:** Apply the general purpose methods for combinational optimization

**CO3:** Understand the concept of Layout Compaction, Placement, Floor planning & Routing, modeling & simulation involved in VLSI system design

**CO4:** Analyze the concept related to synthesis & verification in VLSI system design

**CO5:** Analyze the design cycle of for FPGA and partitioning-routing concepts related to it.

**CO6:** Explain the algorithms for partitioning, floor planning, placement and routing the MCM modules

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COURSE OBJECTIVES:
- To introduce students to the modern embedded systems and to show how to understand and program such systems using a concrete platform built around a modern embedded processor like the Intel ATOM.
- To introduce the students to Embedded Firmware.
- To understand the concepts of RTOS based embedded design.

UNIT –I: Introduction to Embedded Systems

UNIT –II: Typical Embedded System:
Core of the Embedded System: General Purpose and Domain Specific Processors, ASICs, PLDs, Commercial Off-The-Shelf Components (COTS), Memory: ROM, RAM, Memory according to the type of Interface, Memory Shadowing, Memory selection for Embedded Systems, Sensors and Actuators, Communication Interface: Onboard and External Communication Interfaces.

UNIT –III: Embedded Firmware:
Reset Circuit, Brown-out Protection Circuit, Oscillator Unit, Real Time Clock, Watchdog Timer, Embedded Firmware Design Approaches and Development Languages.

UNIT –IV: RTOS Based Embedded System Design:
Operating System Basics, Types of Operating Systems, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling.

UNIT –V:
Task Communication: Shared Memory, Message Passing, Remote Procedure Call and Sockets, Task Synchronization: Task Communication/Synchronization Issues, Task Synchronization Techniques, Device Drivers, How to Choose an RTOS.

TEXT BOOKS:

REFERENCE BOOKS:
1. Embedded Systems – Raj Kamal, TMH.

COURSE OUTCOMES:
Upon completion of this course, students should demonstrate the ability to:
- CO1: Know the Basic Concept of Embedded Systems.
- CO2: CO1: Understand the core of typical embedded system
- CO3: Know the embedded firmware
- CO4: Get introduced to RTOS based Embedded system design & related mechanism
- CO5: Appreciate the methods for task communication for the development of a typical embedded system

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M. TECH- I Semester

COURSEOBJECTIVES:
- To make the student understand how MOSFET and other semiconductor devices are modelled
- To impart knowledge to simulate MOSFET for various operational requirements.
- To impart a knowledge on advanced structures of MOSFETs like SOIFET, FinFET etc.

UNIT -I:
**Introduction to Semiconductor Physics:**
Review of Quantum Mechanics, Boltzman transport equation, Continuity equation, Poisson equation.

**Integrated Passive Devices:**
Types and Structures of resistors and capacitors in monolithic technology, Dependence of model parameters on structures

UNIT -II: **Integrated Diodes**:
Junction and Schottky diodes in monolithic technologies – Static and Dynamic behavior – Small and large signal models – SPICE models

**Integrated Bipolar Transistor:**
Types and structures in monolithic technologies – Basic model (Eber-Moll) – Gunmel - Poon model-dynamic model, Parasitic effects – SPICE model –Parameter extraction

UNIT -III:
**Integrated MOS Transistor:**
NMOS and PMOS transistor – Threshold voltage – Threshold voltage equations – MOS device equations – Basic DC equations second order effects – MOS models – small signal AC characteristics – MOS FET SPICE model level 1, 2, 3 and 4

UNIT -IV:
**VLSI Fabrication Techniques:** An overview of wafer fabrication, Wafer Processing – Oxidation – Patterning – Diffusion – Ion Implantation – Deposition –Silicon gate nMOS process
- CMOS processes – n-well- p-well- twin tub- Silicon on insulator – CMOS process enhancements
- Interconnects circuit elements

UNIT -V:
**Modeling of Hetero Junction Devices:** Band gap Engineering, Band gap Offset at abrupt Hetero Junction, Modified current continuity equations, Hetero Junction bipolar transistors (HBTs),SiGe

TEXT BOOKS:

REFERENCE BOOKS:
COURSE OUTCOMES:
Upon completion of this course, students should demonstrate the ability to:

**CO1:** Understand the physics of and design elements of silicon MOSFETs.

**CO2:** Understand & study the physics behind the operation of integrated diodes & integrated bipolar transistor.

**CO3:** Analyze & study the physics behind the operation of integrated diodes & integrated bipolar transistor.

**CO4:** Understand the VLSI fabrication techniques

**CO5:** To design circuits using Hetero Junction Devices with physical insight of their functional characteristics

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Course Objectives:
- To understand the nuances of language and vocabulary in writing a Research Paper.
- To develop the content, structure and format of writing a research paper.
- To give the practice of writing a Research Paper.
- To enable the student to evolve original research papers without subjected to plagiarism.

UNIT I

UNIT II
RESEARCH FORMAT: Title – Abstract – Introduction – Discussion - Findings – Conclusion – Style of Indentation – Font size/Font types – Indexing – Citation of sources.

UNIT III

UNIT IV

UNIT V
HOW TO & WHERE TO GET PUBLISHED: Reputed Journals – National/International – ISSN No, No. of volumes, Scopes Index/UGC Journals – Free publications - Paid Journal publications – Advantages/Benefits

TEXTBOOKS:

REFERENCES:
1. NPTEL: https://onlinecourses.nptel.ac.in/noc18_mg13/preview

COURSE OUTCOMES:
Upon completion of this course, students should demonstrate the ability to:
- Understand the nuances of language and vocabulary in writing a Research Paper
CO1: Develop the content, structure and format of writing a research paper
CO2: Understand the research methodology in research paper writing
CO3: Analyze and practice writing a Research Paper
CO4: Know how to & where to get published the research work
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M. TECH- I Semester

Course Objectives:
- To develop an understanding of IPR/research methodology in the process of creation of patents through research.
- To develop further research capabilities.
- To learn better report writing skills and Patenting.

UNIT I
RESEARCH METHODOLOGY: Objectives and Motivation of Research, Significance of Literature review, Types of Research, Research Approaches, and Research Methods verses Methodology, Research and Scientific Method, Importance of Research Methodology, Research Process, Criteria of Good Research.

UNIT II

UNIT III

UNIT IV

UNIT V

TEXT BOOKS:

REFERENCES:
COURSE OUTCOMES:
Upon completion of this course, students should demonstrate the ability:

- **CO1**: Appreciate the flow of research methodologies in the research work
- **CO2**: Design Important Concepts Related to Research Design
- **CO3**: Learn better report writing skills and Patenting.
- **CO4**: To write a Research Proposal and Research Report & Research Grant Proposal.
- **CO5**: Understand the importance of Intellectual Property
- **CO6**: To apply for patents
M.Tech- VLSI System Design

VAAGDEVI COLLEGE OF ENGINEERING
(AUTONOMOUS)

(M20VL09) HDL PROGRAMMING LABORATORY

M. TECH- I Semester

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Note: Any 10 of the following digital/analog circuits are to be designed and implemented using Xilinx/Altera/Equivalent CAD tools.

Programming can be done using any complier. Download the programs on FPGA/CPLD boards and performance testing may be done apart from verification by simulation with any of the front end tools.

COURSE OBJECTIVES:

- To design Various Combinational and Sequential circuits using VHDL
- To design Various Combinational and Sequential circuits using Verilog HDL
- To verify different logic circuits using FPGA/CPLD Boards.

List of Experiments:

1. Design and Simulate Combinational circuits in all three modeling of VHDL
2. Design and Simulate 4-bit adder in structural and behavioral modeling VHDL
3. Design and Simulate sequential circuits using VHDL.
4. Design and Simulate State machine using VHDL.
5. Design and Simulate Traffic Light Controller using VHDL.
7. Design and Simulate ALU using Packages and user defined datatype.
8. Design and Simulate Flip-flops using VHDL
9. Design and Simulate Combinational circuits using Verilog HDL
10. Design and Simulate Sequential circuits using Verilog HDL
11. Design and Simulate logic gates using Switch level modeling
12. FPGA implementation of combinational circuit using VHDL and Verilog HDL

COURSE OUTCOMES:

Upon completion of this course, students should demonstrate the ability:

- **CO1**: Apply the knowledge in Simulation and Synthesis of Digital Circuits.
- **CO2**: Design Various Combinational and Sequential circuits using Verilog HDL & HDL
- **CO3**: Explain the System Modeling with Tasks and Functions.
- **CO4**: Design of digital circuits using FPGA/CPLD boards.

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Department of ECE

19
M.Tech-VLSI System Design
VAAGDEVI COLLEGE OF ENGINEERING
(AUTONOMOUS)
(M20VL10)DIGITAL IC DESIGN LABORATORY

M. TECH- I Semester

Note: Any 10 of the following digital/analog circuits are to be designed and implemented using Mentor Graphics / Tanner Tools/Microwind-DSCH/Equivalent CAD tools.

COURSE OBJECTIVES:
- To design Various Combinational circuits using CMOS Logic.
- To design Various Sequential circuits using CMOS Logic.
- To design Various circuits using Different Logic Styles.
- To design Layout of Different logic circuits.

List of Experiments:

1. Design and Simulation of CMOS/NMOS Inverter.
2. Design and Simulation of CMOS Universal Gates.
3. Design and Simulation of Full Adder and Full Subtractor.
4. Design and Simulation of Domino Logic and NORA Logic.
5. Design and Simulation of Dynamic Logic and Pseudo NMOS Logic.
6. Design and Simulation of Transmission Gate and Pass Transistor Logic.
7. Design and Simulation of Bi-CMOS Inverter.
8. Design and Simulation of Bi-CMOS NAND/NOR Logic.
9. Design and Simulation of SRAM Design.
10. Design and Simulation DRAM Design.
11. Post Layout Simulation CMOS Inverter.

COURSE OUTCOMES:
CO1: Design CMOS inverters, logic circuits and transmission gates to specifications.
CO2: Design latches and flip-flops as the basic circuit for Random-Access- Memory (RAM) and Read-Only-Memory (ROM)cells.
CO3: Understand the Design of Bi-CMOS Inverter, logic circuits.
CO4: Design post Layout of Different logic circuits.

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M.Tech—VLSI System Design  
VAAGDEVI COLLEGE OF ENGINEERING  
(AUTONOMOUS)  
(M20VL11)CMOS MIXED SIGNAL CIRCUIT DESIGN

M. TECH- II Semester  
L/T/P/C  
3/0 /0 /3

COURSE OBJECTIVES:
- To know mixed signal circuits like DAC, ADC, PLL etc.
- To gain knowledge on filter design in mixed signal mode.
- To acquire knowledge on design different architectures in mixed signal mode.

UNIT -I:
Switched Capacitor Circuits:
Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing, biquadfilters.

UNIT -II:
Phased Lock Loop (PLL):
Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs-PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications.

UNIT -III:
Data Converter Fundamentals:
DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters

UNIT -IV:
Nyquist Rate A/D Converters:

UNIT -V:
Oversampling Converters:
Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multibit quantizers, Delta sigma D/A

TEXT BOOKS:

REFERENCE BOOKS:
COURSE OUTCOMES:
After completing this course, the students should be able to:

CO1: Build mixed signal circuits like DAC, ADC, PLL etc & Gain knowledge on filter design in mixed signal mode & to acquire knowledge on design different architectures in mixed signal mode.

CO2: Analyze digital test and linear test engineers to the mixed signal world by teaching the basics of analog and mixed signal test methods. Sampling Theory, Frequency Domain Testing, and Digital Signal Processing

CO3: Apply these fundamental concepts to different test methods and data validation for mixed signal parameters together with debugging, noise reduction and device interface techniques.

CO4: Deal with the theory and design skills of switched capacitor circuits, sample-and-hold circuits, and A/D & D/A converters used in modern communication systems and consumer electronic products.

CO5: Design of core mixed-signal IC blocks: comparators and data converters & System level design flow: top-down and bottom-up design methodologies

*****
VAAGDEVI COLLEGE OF ENGINEERING
(AUTONOMOUS)

(M20VL12)VLSI DESIGN VERIFICATION AND TESTING

M. TECH- II Semester

L/T/P/C
3/0 /0 /3

COURSE OBJECTIVES:
- To gain knowledge on digital testing as applied to VLSI design.
- To acquire knowledge on testing of algorithms for digital circuits.
- To learn various testing methods for digital circuits.

UNIT -I: Introduction to Testing:

UNIT -II: Logic and Fault Simulation:

UNIT -III: Testability Measures:
SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

UNIT -IV: Built-In Self-Test:
The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per-Scan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST.

UNIT -V: Boundary Scan Standard:
Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

TEXT BOOKS:

REFERENCE BOOKS:

COURSE OUTCOMES:
After completing this course the students should be able to:

CO1: Understand the need for testing in VLSI & different testing issues
CO2: Gain the knowledge of testing and verification in VLSI design process, ATPG concepts for combinational and sequential circuits
CO3: Apply knowledge of testability measures for testing of digital systems
CO4: Apply knowledge of test-pattern generation & Design for testability techniques for testing of digital systems
CO5: Understanding boundary scan standards & testing techniques for CMOS IC’s
M.Tech-VLSI System Design

VAAGDEVI COLLEGE OF ENGINEERING
(AUTONOMOUS)

(M20VL13) LOW POWER VLSI DESIGN
(Program Elective – III)

M. TECH- II Semester L/T/P/C

3/0 /0 /3

COURSE OBJECTIVES:
➢ To design Low power CMOS designs, for digital circuits.
➢ To gain knowledge on low power circuit design styles for VLSI circuits.
➢ To understand power estimation and optimization methods for VLSI circuits.

UNIT –I: Fundamentals:

UNIT –II: Low-Power Design Approaches:

Switched Capacitance Minimization Approaches:
System Level Measures, Circuit Level Measures, Mask level Measures.

UNIT –III: Low-Voltage Low-Power Adders:

UNIT –IV: Low-Voltage Low-Power Multipliers:
Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh- Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

UNIT –V: Low-Voltage Low-Power Memories:

TEXT BOOKS:
2. Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering.

COURSE OUTCOMES:
After completing this course, the students should be able to:

CO1: Understand the need for low power circuit design & sources of power dissipation in VLSI system

CO2: Appreciate the concept of Low-Power Design Approaches in VLSI system design

CO3: Design low voltage low power adders for given performance specification

CO4: Optimize the power of multiplier using different strategies at different levels of design

CO5: Design low-power CMOS memories using various strategies at different design level

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M.Tech-VLSI System Design

VAAGDEVI COLLEGE OF ENGINEERING
(AUTONOMOUS)

(M20VL14) OPTIMIZATION TECHNIQUES IN VLSI DESIGN
(Program Elective – III)

M. TECH- II Semester

COURSE OBJECTIVES:
- To gain knowledge on Optimization techniques involved in VLSI circuits.
- To explore various Statistical modeling and performance analysis of VLSI Circuits.
- To understand the Concept of Genetic Algorithms and Routing Procedures.

UNIT –I:
Statistical Modeling:
Modeling sources of variations, Monte Carlo techniques, Process variation modeling- Pelgrom’s model, Principle component-based modeling, Quad tree based modeling, Performance modeling- Response surface methodology, delay modeling, interconnect delay models.

UNIT –II:
Statistical Performance, Power and Yield Analysis
Statistical timing analysis, parameter space techniques, Bayesian networks Leakage models, High level statistical analysis, Gate level statistical analysis, dynamic power, leakage power, temperature and power supply variations, High level yield estimation and gate level yield estimation.

UNIT –III:
Convex Optimization:
Convex sets, convex functions, geometric programming, trade-off and sensitivity analysis, Generalized geometric programming, geometric programming applied to digital circuit gate sizing, Floor planning, wire sizing, Approximation and fitting- Monomial fitting, Maxmonomial fitting, Posynomial fitting.

UNIT –IV:
Genetic Algorithm:

UNIT –V:
GA Routing Procedures and Power Estimation:

TEXT BOOKS / REFERENCE BOOKS:
COURSE OUTCOMES:

After completing this course, the students should be able to:

**CO1:** Gain knowledge on Optimization techniques involved in VLSI circuits.

**CO1:** Analyze methods of optimization to engineering students, including linear programming, nonlinear programming, and heuristic methods.

**CO1:** Understand balance between theory, numerical computation, problem setup for solution by optimization software, and applications to engineering systems.

**CO1:** Studies General optimization algorithm; necessary and sufficient conditions for optimality.

**CO1:** Demonstrate the Concept of Genetic Algorithms and Routing Procedures.

***
COURSE OBJECTIVES:
➢ To gain knowledge on circuits and techniques involved in high speed VLSI circuits.
➢ To explore various design strategies to be followed for designing a high speed VLSI circuit.
➢ To understand the logic styles for designing a high speed VLSI circuit.

UNIT I - CLOCKED LOGIC STYLES:
Clocked Logic Styles, Single-Rail Domino Logic Styles, Dual-Rail Domino Structures, Latched Domino Structures, Clocked pass Gate Logic Non-Clocked Logic Styles, Static CMOS, DCVS Logic, Non-Clocked pass Gate Families.

UNIT II - CIRCUIT DESIGN MARGINING AND DESIGN VARIABILITY:
Circuit Design Margining, Design Induced Variations, Process Induced Variations, Application Induced Variations, Noise.

UNIT III - LATCHING STRATEGIES:

UNIT IV - INTERFACE TECHNIQUES:
Signaling Standards, Chip-to-Chip Communication Networks, ESD Protection, Skew Tolerant Design

UNIT V - CLOCKING STYLES:
Clocking Styles, Clock Jitter, Clock Skew, Clock Generation, Clock Distribution, Asynchronous Clocking Techniques.

REFERENCES

COURSE OUTCOMES:
After completing this course, the students should be able to:
CO1: Appreciate the different clocking logic styles in VLSI system design as per specification
CO2: Understand circuit design margining & design variability for VLSI circuit
CO3: Appreciate the concept of latching strategies to optimize the speed of the system
CO4: Gain knowledge on interface techniques involved in high speed VLSI circuits.
CO5: Analyze the clocking styles in design to optimize the timing issues to support high speed processing
COURSE OBJECTIVES:
➢ To learn the fundamentals of ASIC and its design methods
➢ To gain knowledge on programmable architectures for ASICs
➢ To understand the physical design of ASIC.

UNIT I - INTRODUCTION TO ASIC’S
Types of ASICs - Design flow - CMOS transistors CMOS Design rules - Combinational Logic Cell - Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort - Library cell design - Library architecture.

UNIT II - PROGRAMMABLE ASIC’S
Anti fuse - static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT - Xilinx LCA -Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs – Xilinx I/O blocks.

UNIT III - PROGRAMMABLE ASIC LOGIC CELLS

UNIT IV - ASIC FLOOR PLANNING, PLACEMENT AND ROUTING

UNIT V - OPTIMIZATION ALGORITHMS
Planar subset problem(PSP) -single layer global routing single layer detailed routing wire length and bend minimization technique -over the cell(OTC) Routing-multichip modules(MCM)- Programmable logic arrays-Transistor chaining-Weinberger Arrays-Gate Matrix Layout-1D compaction-2Dcompaction

REFERENCES

COURSE OUTCOMES:
After completing this course, the students should be able to
CO1: To learn the fundamentals of ASIC and its design methods
CO2: To gain knowledge on programmable architectures for ASICs & physical design of ASIC
CO3: Understand the programmable ASIC Logic Cells & selection of suitable ASIC Logic cells for design
CO4: Analyze ASIC floor planning, placement and routing in VLSI Design
CO5: Appreciate concept of optimization algorithms in the design of an efficient layout.
M. TECH- II Semester

L/T/P/C
3/0 /0 /3

COURSE OBJECTIVES:
➢ To learn System on chip fundamentals, their applications.
➢ To gain knowledge on SOC design.
➢ To learn the various computation models of SOCs.

UNIT –I:
Introduction to the System Approach:

UNIT –II:
Processors:

UNIT –III:
Memory Design for SOC:

UNIT -IV:
Interconnect Customization and Configuration:

UNIT –V:
Application Studies / Case Studies:
SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.

TEXT BOOKS:

REFERENCE BOOKS:
2. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM.

COURSE OUTCOMES:
After completing this course, the students should be able to:

CO1: Apply the knowledge of SoC architecture & organization
CO2: Analyze various processor microarchitecture & design trade-off for SoC
CO3: Understand the memory design for SoC
CO4: Evaluate interconnect structure for different topologies
CO5: Design Soc based Embedded system on FPGA
VAAGDEVI COLLEGE OF ENGINEERING
(AUTONOMOUS)
(M20VL18)SEMICONDUCTOR MEMORY DESIGN AND TESTING
(Program Elective – IV)

M. TECH- II Semester

COURSE OBJECTIVES:
- To know the design of MOS memories and the various precautionary methods to be used in their design.
- To gain knowledge on various testing methods of semiconductor memories.
- To get an overview on reliability of semiconductors and their testing.

UNIT –I Random Access Memory Technologies:
SRAM – SRAM Cell structures, MOS SRAM Architecture, MOS SRAM cell and peripheral circuit operation, Bipolar SRAM technologies, SOI technology, Advanced SRAM architectures and technologies, Application specific SRAMs, DRAM – DRAM technology development, CMOS DRAM, DRAM cell theory and advanced cell structures, BICMOS DRAM, soft error failurein DRAM, Advanced DRAM design and architecture, Application specific DRAM

UNIT –II Non-volatile Memories:
Masked ROMs, High density ROM, PROM, Bipolar ROM, CMOS PROMS, EPROM, Floating gate EPROM cell, One time programmable EPROM, EEPROM, EEPROM technology and architecture, Non-volatile SRAM, Flash Memories (EPROM or EEPROM), advanced Flash memory architecture

UNIT -III:
Memory Fault Modeling Testing and Memory Design for Testability and Fault Tolerance:
RAM fault modeling, Electrical testing, Pseudo Random testing, Megabit DRAM Testing, non-volatile memory modeling and testing, IDDQ fault modeling and testing, Application specific memory testing, RAM fault modeling, BIST techniques for memory

UNIT -IV:
Semiconductor Memory Reliability and Radiation Effects:
General reliability issues RAM failure modes and mechanism, Non-volatile memory reliability, reliability modeling and failure rate prediction, Design for Reliability, Reliability Test Structures, Reliability Screening and qualification, Radiation effects, Single Event Phenomenon (SEP), Radiation Hardening techniques, Radiation Hardening Process and Design Issues, Radiation Hardened Memory characteristics, Radiation Hardness Assurance and Testing, Radiation Dosimetry, Water Level Radiation Testing and Test structures

UNIT -V:
Advanced Memory Technologies and High-density Memory Packing Technologies:
Ferroelectric RAMs (FRAMs), GaAs FRAMs, Analog memories, magneto resistive RAMs (MRAMs), Experimental memory devices, Memory Hybrids and MCMs (2D), Memory Stacks and MCMs (3D), Memory MCM testing and reliability issues, Memory cards, High Density Memory Packaging Future Directions

TEXT BOOKS:
COURSE OUTCOMES:
After completing this course, the students should be able to:
CO1: Know the design of MOS memories and the various precautionary methods to be used in their design
CO2: Learn overview of memory chip design, DRAM circuits, voltage generators, performance analysis and design issues of ultra-low voltage memory circuits
CO3: Acquire knowledge about High-Performance Subsystem Memories & Analyse RAM and DRAM Design
CO4: Demonstrate Advanced Memory Technologies and High-density Memory Packing Technologies & Gains knowledge on various testing methods of semiconductor memories
CO5: Get an overview on reliability of semiconductors and their testing

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VAAGDEVI COLLEGE OF ENGINEERING
(AUTONOMOUS)

(M20AC02) STRESS MANAGEMENT

M. TECH- II Semester

Course Objectives:
- This course provides understanding stress such as work related stress and individual stress
- This course serves time management such as importance of planning the day and developing concentration
- This course serves career plateau such as Identifying Career plateaus and Structural and Content Plateauing and Making a fresh start
- This course provides controlling crisis management
- This course provides self development

UNIT – I UNDERSTANDING STRESS

UNIT – II TIME MANAGEMENT
Techniques – Importance of Planning the day –developing concentration – Prioritizing Beginning at the start – Techniques for conquering procrastination – Sensible delegation – Taking the right breaks – Learning to say“No”

UNIT – III CAREER PLATEAU

UNIT – IV CRISIS MANAGEMENT

UNIT – V SELF DEVELOPMENT
Improving personality – Leading with Integrity – Enhancing Creativity – Effective decision making – Sensible Communication – The Listening Game – Managing Self – Mediation for peace – Yoga for Life

TEXT BOOKS

REFERENCES
1. Jeffr Davison, Managing Stress, Prentice Hall of India, NewDelhi

COURSE OUTCOMES:
- CO1: Enhance of Physical strength and flexibility.
- CO2: Learn to relax and focus.
- CO3: Relieve physical and mental tension
- CO4: Improve work performance/efficiency.
Note: Any 10 of the following digital/analog circuits are to be designed and implemented using Mentor Graphics / Tanner Tools/Microwind-DSCH/NG-Spice/Equivalent CAD tools.

COURSE OBJECTIVES:

- To design Various Characteristics of MOS Logic.
- To design Various Amplifier circuits using CMOS Logic.
- To design Various circuits using Different Logic Styles.
- To design Layout of Different logic circuits.

List of Experiments:

1. Design of DC Characteristics of MOS Transistor.
2. Design and simulation of MOS current sources and current mirrors.
3. Design and simulation of emitter follower circuit.
5. Design and simulation of Clippers and Clampers
7. Design and simulation of any circuit using current sink load.

COURSE OUTCOMES:

After completing this course the students should be able to:

CO1: Design Various Characteristics of MOS Logic
CO2: Design Various Amplifier circuits using CMOS Logic
CO3: Design Various circuits using Different Logic Styles
CO4: Design Layout of Different logic circuits

*****
M.Tech-VLSI System Design

VAAGDEVI COLLEGE OF ENGINEERING
(AUTONOMOUS)

(M20VL20) MIXED SIGNAL VLSI LABORATORY

M. TECH- II Semester

L/T/P/C
0/0 /4 /2

Note: Any 10 of the following digital/analog circuits are to be designed and implemented using Mentor Graphics / Tanner Tools/Microwind-DSCH/NG-Spice/Equivalent CAD tools.

COURSE OBJECTIVES:

- To design Various Amplifier circuits using CMOS Logic
- To design Various Complex circuits using Different Logic Styles
- To design Layout of Different logic circuits

List of Experiments:

1. SPICE simulation of Cascode Amplifier.
2. SPICE simulation of Differential Amplifier using Switched capacitor.
3. SPICE simulation of Two stage Operational Amplifier.
4. SPICE simulation of Two stage Comparator Circuit
5. SPICE simulation of Inverting Amplifier.
6. SPICE simulation Sample and Hold Circuit.
7. SPICE simulation of PLL.
8. SPICE simulation of Latches/Flip flops using CMOS.
9. SPICE simulation of Combinational Circuit using Bi-CMOS Logic.
10. Post Layout Simulation of Combinational Circuit
11. Post Layout Simulation of Sequential Circuit.

COURSE OUTCOMES:

After completing this course, the students should be able to:

CO1: Design Various Amplifier circuits using CMOS Logic
CO2: Design Various Complex circuits using Different Logic Styles
CO3: Design Layout of Different logic circuits
CO4: Digital/analog circuits are to be designed and implemented using CAD tools.

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M.Tech-VLSI System Design

VAAGDEVI COLLEGE OF ENGINEERING
(AUTONOMOUS)

(M20VL21) MINI PROJECT

M. TECH- II Semester

COURSE OUTCOMES:

After the completion of this course, the students should be able to

- Use fundamental knowledge and skills in engineering and apply it effectively on a project.
- Understand the Product Development Process including budgeting through Mini Project.
- Plan for various activities of the miniproject.
- Inculcate electronic hardware and software implementation skills.
- Manage any disputes and conflicts within and outside individually.
- Prepare a technical report based on the Miniproject.
- Deliver technical seminar based on the Mini Project work carried out.
COURSE OBJECTIVES:

- To know the various methods for implementation of DSP systems.
- To understand the various implementations of VLSI DSP architectures for Arithmetic operations
- To gain knowledge on low power DSP architectures.

UNIT I – UNFOLDING:

UNIT II - DIGITAL MULTIPLIER ARCHITECTURES:
Parallel Multipliers- Interleaved Floor-plan and Bit-Plane-Based Digital Filters- Bit-Serial Multipliers- Bit-serial Filter Design and Implementation, Canonic Signed Digit Arithmetic- Distributed Arithmetic.

UNIT III - REDUNDANT ARITHMETIC:

UNIT IV - SYNCHRONOUS AND ASYNCHRONOUS PIPELINING:
Synchronous Pipelining and Clocking Styles- Clock Skew and Clock Distribution in Bit-Level Pipelined VLSI Designs- Wave Pipelining Constraint Space Diagram and Degree of Wave Pipelining- Implementation of Wave-Pipelined Systems- Asynchronous Pipelining- Signal Transition Graphs- Use of STG to Design Interconnection Circuits- Implementation of Computational Units.

UNIT V - LOW POWER VLSI DSP SYSTEMS:
Theoretical Background- Scaling Versus Power Consumption- Power Analysis- Power Reduction Techniques- Power Estimation Approaches.- Simulation Based Approach.

REFERENCES

COURSE OUTCOMES:
After completing this course the students should be able to:

CO1: Apply the concept of unfolding for optimization of critical paths in the VLSI system design
CO2: Design Multiplier architectures in optimized way for given specification in VLSI Design
CO3: Apply the redundant arithmetic for optimization of adder & multiplier block generally
M.Tech-VLSI System Design
used in digital signal processing application

**CO4:** Analyze the use of synchronous & asynchronous pipelining in to optimize the performance of High Speed VLSI Design

**CO5:** Understand the low power VLSI DSP system

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COURSE OBJECTIVES:

- To learn the various limitation on MOSFETS and the alternates.
- To gain knowledge on SET and Carbon nanotubes in the design of transistors
- To learn the basics of molecular electronics and spintronics.

UNIT I - LIMITATION OF MOSFETS:
Classical mechanics and its drawbacks, Quantum mechanics, 1D problem - particle in a box, electron tunneling, MOSFET scaling, Non-uniform doping in channel, high K dielectrics, SOI MOSFET, Buried channel MOSFET, Fin FET.

UNIT II - SINGLE ELECTRONICS:
Coulomb blockade, Electron tunneling devices, Single electron transistors, Resonant Tunneling Diodes- principle and applications, Quantum computing, Quantum cellular automata

UNIT III- CARBON NANO TUBES:
Carbon nano tubes – Basic structures, CNTFETs, Applications.

UNIT IV - MOLECULAR ELECTRONICS:
Molecular wire conductance - Theories of Coherent Electron Transport in molecular junctions, Evaluation of the conductance for coherent transport, Incoherent transport and vibrionic coupling, Molecular circuit elements, Circuits.

UNIT V – SPINTRONICS:
Spin Vs charge, AMR, GMR, TMR, Spin devices- Spin valves, Magnetic tunnel junctions, Applications – memories (MRAM, STRAM), Logic device, and microwave oscillators.

REFERENCES:

COURSE OUTCOMES:
After completing this course the students should be able to:

CO1: Understand the limitations of the MOSFETs & potential of nanoelectronics

CO2: Show a deeper understanding of the relation between novel behavior of nanoelectronics devices and quantum behavior of the matter at the nano scale as well as the breakdown of received scaling wisdom

CO3: Understand structures of carbon nanotubes & its applications

CO4: Appreciate the concept of molecular electronics in nanoscale fabrication technologies understand the principle of spintronic
M.Tech- III Semester  
L/T/P/C   3/0/0/3

COURSE OBJECTIVES:
➢ To explore the various performance measures of RF circuits.
➢ To acquire knowledge on the design of RF filters, amplifiers and oscillators.

UNIT I - PERFORMANCE PARAMETERS OF RFCIRCUITS:
Gain Parameters, Non-linearity parameters, Noise figure, Phase Noise, Dynamic range, RF front end performance parameters, performance trade-offs in an RF circuit.

UNIT II - FILTER DESIGN:
Modern filter design, Frequency and impedance scaling, High Pass filter design, Band pass filter design, Band reject filter design, the effects of finite Q.

UNIT III - HIGH FREQUENCY AMPLIFIER DESIGN:
Zeros as Bandwidth enhances, Shunt-series Amplifier, Bandwidth enhancement with frequency Doublers, Tuned amplifiers, Neutralization and unilateralization, cascaded Amplifiers, LNA Topologies.

UNIT IV - MIXERS AND OSCILLATORS:
Mixer fundamentals, Nonlinear systems as Linear mixers, multiplier based mixers, Subsampling mixers. Problems with purely linear oscillators, Tuned oscillator, Negative Resistance oscillators, frequency synthesis.

UNIT V - RF POWER AMPLIFIERS:
General considerations, Class A, AB, B & C Power amplifier, Class D, E & F amplifiers, modulation of power amplifiers, RF Power amplifier design examples.

REFERENCES:

COURSE OUTCOMES:
After completing this course the students should be able to:
CO1: Understand the performance parameters / specifications of the RF Circuits
CO2: Design & analyze the filter design
CO3: Understand & evaluate the performance of various specifications of high frequency amplifier design, Mixer, Oscillators & Power Amplifiers
CO4: Understand the source of nonlinearity, noise, process technology & its impact on the parameters of individual blocks of receiver & on receiver performance
CO5: Demonstrate the tools & techniques to evaluate the performance specifications of the RF building blocks

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M. TECH- III Semester

COURSE OBJECTIVES:

- To understand the concepts of soft computing techniques.
- To enable to develop applications of soft computing in real life problems.

UNIT – I: Fundamentals of Neural Networks & Feed Forward Networks
Basic Concept of Neural Networks, Human Brain, Models of an Artificial Neuron, Learning Methods, Neural Networks Architectures, Signal Layer Feed Forward Neural Network :The Perceptron Model, Multilayer Feed Forward Neural Network :Architecture of a Back Propagation Network (BPN), The Solution, Back propagation Learning, Selection of various Parameters in BPN. Application of Back propagation Networks in Pattern Recognition & Image Processing.

UNIT – II: Associative Memories & ART Neural Networks
Basic concepts of Linear Associator, Basic concepts of Dynamical systems, Mathematical Foundation of Discrete-Time Hop field Networks (HPF), Mathematical Foundation of Gradient-Type Hopfield Networks, Transient response of Continuous Time Networks, Applications of HPF in Solution of Optimization Problem: Minimization of the Traveling salesman tour length, Summing networks with digital outputs, Solving Simultaneous Linear Equations, Bidirectional Associative Memory Networks; Cluster Structure, Vector Quantization, Classical ART Networks, Simplified ART Architecture.

UNIT – III: Fuzzy Logic & Systems
Fuzzy sets, Crisp Relations, Fuzzy Relations, Crisp Logic, Predicate Logic, Fuzzy Logic, Fuzzy Rule based system, Defuzzification Methods, Applications: Greg Viot’s Fuzzy Cruise Controller, Air Conditioner Controller.

UNIT – IV: Genetic Algorithms

UNIT – V: Hybrid Systems

TEXT BOOKS:
1. Introduction to Artificial Neural Systems – J.M.Zurada, Jaico Publishers

REFERENCE BOOKS:
1. Artificial Neural Networks- Dr. B. Yagananarayana, 1999, PHI, New Delhi.
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COURSE OUTCOMES:

After completing this course, the students should be able to:

- Understand the Fundamentals of Neural Networks & Feed Forward Networks
- Design & analyze the Associative Memories & ART Neural Networks
- Understand & evaluate the performance of Fuzzy Logic & Systems
- Understand the Genetic Algorithms
- Design & analyze Hybrid Systems
- Understand Soft Computing concepts, technologies, and applications
- Understand the underlying principle of soft computing with its usage in various applications

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COURSE OBJECTIVES:
- To impart a knowledge on basics of graph theory and its algorithms
- To impart a knowledge on basic optimization techniques.
- To impart a knowledge on various statistical methods in analyzing a sample.

UNIT –I BASICS OF GRAPH THEORY:

UNIT –II CLASSES OF GRAPH:
Eulerian graphs and Hamiltonian graphs - standard theorems- planar graphs Euler’s formula – five color problem- coloring of graphs- chromatic number (vertex and edge) properties and examples- directed graphs

UNIT –III GRAPH ALGORITHMS:
Computer representation of graphs-Basic graph algorithms- minimal spanning tree algorithm - Kruskal and prim’s algorithm- shortest path algorithms- Dijkstra’s algorithm- DFS and BFS algorithms.

UNIT –IV OPTIMIZATION TECHNIQUES:
Linear programming- graphical methods- simplex method (Artificial variables not included) - transportation and assignment problems.

UNIT –V STATISTICS:
Tchebyshev’s inequality – Maximum likelihood estimation- correlation partial correlation- multiple correlations- regression- Multiple regressions.

REFERENCES:

COURSE OUTCOMES:
After completing this course the students should be able to:
- Understand the various types of graph Algorithms and graph theory properties.
- Analyze the NP – complete problems.
- Distinguish the features of the various tree and matching algorithms
- Appreciate the applications of digraphs and graph flow
- Understand the linear programming principles and its conversion
- Design and employ appropriate method for solving computing problems

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M.Tech-VLSI System Design
VAAGDEVI COLLEGE OF ENGINEERING
(AUTONOMOUS)
(M20SE27) WASTEMANAGEMENT

M. TECH- III Semester

COURSE OBJECTIVES:

- To assess the activities involved for the proposed and determine the type, nature and estimated volumes of waste to be generated.
- To identify any potential environmental impacts from the generation of waste at the site.
- To recommend appropriate waste handling and disposal measures

Unit - I Introduction to Environment:

Unit - II Municipal solid waste:

Unit - III Collection and Transfer Collection:

Unit – IV Processing Techniques and Recovery of Energy:

Unit – V Disposal of Solid Wastes:

References:
5. Ecology Science and Practice; Claude Fourie, Christian Ferra, Paul Medori, TeanDevaux,
COURSE OUTCOMES:

- Understand how waste management practices protect environmental health and safety.
- Apply physical and chemical analysis on municipal solid wastes.
- Enhance the route for solid waste collection and transport system.
- Develop a method to use energy from solid wastes.
- Explain different methods of disposal of hazardous solid waste.

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COURSE OUTCOMES:

After the completion of this course, the students should be able to

- Use specialized knowledge and skills in engineering and apply it effectively on a project.
- Apply knowledge of the ‘real world’ situations that a professional engineer can encounter.
- Apply critical and creative thinking in the design of VLSI System Design projects.
- Demonstrate a sound technical knowledge of selected project topic.
- Demonstrate the skills and attitude of a professional engineer.
- Summarize an appropriate list of literature review, analyse previous work and relate them to current project.
- Deliver technical seminar based on the Project work carried out.
- Publish the conducted research work in a National / International Conference or Journal preferably IEEE, ACM, Springer and Scopus indexed/SCI indexed/ESCI.