VAAGDEVI COLLEGE OF ENGINEERING

Autonomous

Bollikunta, Khila Warangal (Mandal), Warangal Urban-506 005 (T.S), www.vaagdevi.edu.in

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Minutes of the meeting of the Board of Studies held on 24-11-2020

The following members were present:

SL.No	Members Present	Designation	Signature
1.	Mr. M. Shashidhar Assoc. Prof., ECE Dept., VCE Warangal. sasi47004@gmail.com	Chairman	
2.	Mrs. T. Madhavi Kumari, Assoc. Prof. & Addl. Controller of Examination,JNTU, Hyderabad. thoomati@jntuh.ac.in, thoomati@gmail.com	JNTUH Nominee	25/11/2020
3.	Dr.Y.Raghavendra Rao, Head of the Department JNTU , Sulthanpur	Subject Expert	25/11/2020
4.	Prof. P. Prasad Rao, Principal, VEC Warangal Principal.vec@gmail.com	Subject Expert	
5.	Mr. P. Rohit, CEO, Suhrud Applab Private limited, Warangal mails2rohith@gmail.com	Industry Representative	email Consent Received
6.	Bala Krishna Islavath, Scientist, R&D, Laboratory Center for Electromagnetic, Ministry of Electronics and Information Technology, Government of India islavath32@@gmail.com	Undergraduate Alumni	email Consent Received
7.	Mr. P. G. Mahesh, Senior Silicon Design Engineer at AMD Goud.mahesh058@live.com	Undergraduate Alumni	
8.	Dr. Jitesh Ramdas Shinde, Asst. Prof, ECE Dept, VCE, Warangal shindejitesh.vaagdevi.coe.ece@gmail.com	Member	

9.	Dr. M. Ranjith, Asst. Prof, ECE Dept, VCE, Warangal ranjithmamidi2001@gmail.com	Member	
10.	Dr. Nishu Gupta, Assoc. Prof. ECE, VCE Warangal gupta_n@vaagdevi.edu.in	Member	

The following decisions are taken:

1. It is resolved to approve the course structure and syllabi of B.Tech Electronics and communication engineering I Semester and II Semester (R20 Regulation from the academic year 2020-2021onwards).

2. The following changes are made

    a) Chemistry syllabus is framed according to the requirement of the domain subjects of the ECE department and is included in the I-semester.

    b) Basic Python programming theory and lab included in II semester to make the students themselves ready to face the challenges of the multinational companies or any industry oriented software jobs.

3. It is resolved to approve the course structure and syllabi of M.Tech-VLSI System Design I & II years (under R20 Regulation from the academic year 2020-2021onwards).

(Chairman-BOS)

VAAGDEVI COLLEGE OF ENGINEERING
(AUTONOMOUS)
B.TECH. ELECTRONICS & COMMUNICATION ENGINEERING

COURSE STRUCTURE
(R20 Regulations applicable for the batches admitted from Academic Year 2020-21)

I SEMESTER

S.No.	Course Code	Title of the Course	L	T	P	Credits
1		Linear Algebra & Calculus	3	1	0	4
2		Programming for Problem Solving	4	0	0	4
3		Modern Physics	3	0	0	3
4		Chemistry	3	0	0	3
5		Engineering Drawing	0	0	4	2
6		Physics Lab	0	0	3	1.5
7		Programming for Problem Solving Lab	0	0	3	1.5
8		Induction Program				
		Total Credits	**13**	**01**	**10**	**19**

II SEMESTER

S.No.	Course Code	Title of the Course	L	T	P	Credits
1		Differential Equations & Vector Calculus	3	1	0	4
2		Basic Electronic devices	3	1	0	4
3		Electrical Circuits	3	0	0	3
4		Basic Python programming	3	0	0	3
5		i-English (Individualized English) Skills Lab	0	0	3	1.5
6		Basic Electronic Devices Lab	0	0	3	1.5
7		Basic Python programming Lab	0	0	3	1.5
8		Engineering & IT Workshop	0	0	3	1.5
9		Sports				
		Total Credits	12	02	12	20

1. 25/11/20
2. 25/11/2020
3. 25/11/2020
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VAAGDEVI COLLEGE OF ENGINEERING
(AUTONOMOUS)
BOLLIKUNTA, WARANGAL
B.TECH. ELECTRONICS & COMMUNICATION ENGINEERING

COURSE STRUCTURE
(R20 Regulations applicable for the batches admitted from Academic Year 2020-21)

III SEMESTER

S.No.	Subject code	Subject	L	T	P	Credits
1		Numerical Methods & Complex Variables	3	1	0	4
2		Signals and Systems	4	0	0	4
3		Electronic Circuits Analysis	3	0	0	3
4		Switching Theory and Logic Design	3	0	0	3
5		Electrical Technology	3	0	0	3
6		Electronic Circuits Analysis Lab	0	0	3	1.5
7		Electronic Simulation EDA Tools Lab	1	0	3	2
8		Electrical Technology Lab	0	0	3	1.5
9		NSS/NCC	0	0	2	0
		Total Credits	**17**	**01**	**11**	**22**

IV SEMESTER

S.No.	Subject code	Subject	L	T	P	Credits
1		Pulse and Digital Circuits	3	0	0	3
2		Analog & Digital Communications	3	0	0	3
3		Electromagnetic Theory and Transmission Lines.	3	0	0	3
4		Probability Theory and Stochastic Process	3	0	0	3
5		Computer Organization	3	0	0	3
6		Pulse and digital circuits Lab	0	0	3	1.5
7		English skills for digital natives	2	0	0	2
8		Analog & Digital Communications lab	0	0	3	1.5
		Total Credits	**17**	**00**	**06**	**20**

Comment [m1]: Is it lab or theory?

1. 28/11/20
2. 25/11/2020
3. 25/11/2020
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Regarding course structure

Inbox

Bobbala Sridevi Thu, Dec 3, 12:26 PM (21 hours ago)

Dear Balakrishna The following course structure is being finalized according to the discussions in B...

Krish Thu, Dec 3, 3:51 PM (17 hours ago)

to me

Approved.

On Thu, 3 Dec, 2020, 12:26 PM Bobbala Sridevi, <vaagvijs15@gmail.com> wrote:

> Dear Balakrishna
> The following course structure is being finalized according to the discussions in Board of studies meeting. kindly find the attachment of the above and approve the same.
>
> B.Sreedevi
> associate professor
> ECE department

Krish Thu, Dec 3, 3:51 PM (17 hours ago)

to me

Approved the above course plan.

.....

Thanks and Regards
Balakrishna Islavath
Scientist
Center for Electromagnetics(R&D Lab)
Ministry of Electronics and Information Technology
Government of India

Thanks a lot. | Thanks for your support. | Thank you for your response.

Reply | Forward

Regarding course structure

Inbox

Bobbala Sridevi Thu, Dec 3, 12:24 PM (21 hours ago)

Dear Rohith The following course structure is being finalized according to the discussions in Board ...

Rohith Pothepalli Thu, Dec 3, 12:30 PM (21 hours ago)

to me

Approved.

On Thu, Dec 3, 2020 at 12:24 PM Bobbala Sridevi <vaagvijs15@gmail.com> wrote:

> Dear Rohith
> The following course structure is being finalized according to the discussions in Board of studies meeting. kindly find the attachment of the above and approve the same.
>
> B.Sreedevi
> associate professor
> ECE department

Rohith Pothepalli Thu, Dec 3, 2:33 PM (18 hours ago)

to me

Good Afternoon Mam,

I acknowledge receipt of your email reagarding finalization of the course structure. As discussed in Board of Studies meeting I approve the course structure.
Thanks for keeping me in the loop.

Regards,
Rohit Potepalli

Noted with thanks. | Thank you for your response. | Thanks a lot.

Reply | Forward

Regarding course structure

Inbox

Bobbala Sridevi Thu, Dec 3, 12:22 PM (21 hours ago)

Dear Mahesh The following course structure is being finalized according to the discussions in Board...

Mahesh Goud Pogakula Thu, Dec 3, 1:31 PM (20 hours ago)

to me

Hi Sridevi Ma'am ,

The Course structure looks good . Kindly, Please go-ahead with same .

Thanks and Regards,
Mahi

From: Bobbala Sridevi <vaagvijs15@gmail.com>
Sent: Thursday, December 3, 2020 6:52 AM
To: Goud.mahesh058@live.com <Goud.mahesh058@live.com>
Subject: Regarding course structure

Dear Mahesh
The following course structure is being finalized according to the discussions in Board of studies meeting. kindly find the attachment of the above and approve the same.

B.Sreedevi
associate professor
ECE department

Sure, will do that. | Thanks a lot. | It is not available.

Reply | Forward

VAAGDEVI COLLEGE OF ENGINEERING

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Bollikunta, Warangal

Department of Electronics & Communication Engineering

M.TECH. (VLSI System Design)

COURSE STRUCTURE

(R20 Regulations applicable for the batches admitted from Academic Year 2020-21 onwards)

I-SEMESTER

S.No.	Course Code	Title of the Course	L	T	P	Credits
1	M20VL01	CMOS Digital Integrated Circuit Design	3	0	0	3
2	M20VL02	CMOS Analog Integrated Circuit Design	3	0	0	3
3	M20VL03 M20VL04 M20VL05	**Program Elective-I** Digital System Design using HDL VLSI Signal Processing VLSI Technology	3	0	0	3
4	M20VL06 M20VL07 M20VL08	**Program Elective-II** Algorithms For VLSI Design Automation Embedded System Design Device Modelling	3	0	0	3
5	M20AC01	English For Research Paper Writing	2	0	0	0
6	M20MC01	Research Methodology	2	0	0	2
7	M20VL09	HDL Programming Laboratory	0	0	4	2
8	M20VL10	Digital IC Design Laboratory	0	0	4	2
		Total Credits	**16**	**00**	**08**	**18**

II-SEMESTER

S.No.	Course Code	Title of the Course	L	T	P	Credits
1	M20VL11	CMOS Mixed Signal Circuit Design	3	0	0	3
2	M20VL12	VLSI Design Verification and Testing	3	0	0	3
3	M20VL13 M20VL14 M20VL15	**Program Elective-III** Low Power VLSI Design Optimization Technique In VLSI Design High Speed VLSI Design	3	0	0	3
4	M20VL16 M20VL17 M20VL18	**Program Elective-IV** ASIC Design System On Chip Architecture Semiconductor Memory Design & Testing	3	0	0	3
5	M20AC02	Stress Management	2	0	0	0
6	M20VL19	Analog IC Design Laboratory	0	0	4	2
7	M20VL20	Mixed Signal VLSI Laboratory	0	0	4	2
8	M20VL21	Mini Project	0	0	4	2
		Total Credits	**14**	**00**	**12**	**18**

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Department of Electronics & Communication Engineering

M.TECH. (VLSI System Design)

COURSE STRUCTURE

(R20 Regulations applicable for the batches admitted from Academic Year 2020-21 onwards)

III-SEMESTER

S.No.	Course Code	Title of the Course	L	T	P	Credits
1		**Program Elective-V**	3	0	0	3
	M20VL22	High Speed VLSI Architectures for DSP Applications				
	M20VL23	Nano materials & Nano Technology				
	M20VL24	RF Circuit Design				
2		**Open Elective**	3	0	0	3
	M20CS12	Soft Computing Techniques				
	M20MA02	Graph Theory & Optimization Techniques				
	M20SE27	Waste Management				
3	M20VL25	Dissertation Phase-I	0	0	20	10
		Total Credits	**06**	**00**	**20**	**16**

IV-SEMESTER

S.No.	Course Code	Title of the Course	L	T	P	Credits
1	M20VL26	Dissertation Phase-II	0	0	32	16
		Total Credits	**00**	**00**	**32**	**16**

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