



Viswambhara Educational Society
VAAGDEVI COLLEGE OF ENGINEERING
Autonomous
P.O. Bollikunta, Warangal – 506 005 (Telangana State)

Department of Electronics & Communication Engineering

Minutes of the meeting of the Board of Studies held on 02-07-2018 at 10:30am.

The following members were present:

| SL.No | Members Present | Designation | Signature |
|-------|--|-------------------------|-----------|
| 1. | Mr. M. Shashidhar Assoc. Prof, Head, ECE Dept, VCE, Warangal | Chairman | |
| 2. | Prof. M. AshaRani , ECE. Dept. | JNTUH Nominee | |
| 3. | Dr. T. Kishore Kumar, Professor, ECE Dept. NIT, Warangal | Subject Expert | |
| 4. | Prof. P. Prasad Rao VEC, Principal, Warangal | Subject Expert | |
| 5. | Mr. P. Rohit, CEO, Suhrud Applab Private limited, Warangal | Industry Representative | |
| 6. | Mr. N. Kiran, JTO BSNL | Postgraduate Alumni | |
| 7. | Mr. K. Srinath, Jr Engg, NPDCL | Postgraduate Alumni | |
| 8. | Dr. Nishu Gupta, Asst. Prof, ECE Dept, VCE, Warangal | Member | |
| 9. | Dr. Jitesh Ramdas Shinde, Asst. Prof, ECE Dept, VCE, Warangal | Member | |

The following decisions are taken:

1. Approved the course structure for B. Tech. I,II, III & IV Years under R18 regulation.
2. Approved the syllabi of B.Tech. (R18-regulation) for I-Year I and II Semesters.
3. Approved the course structure and syllabus for M.Tech (VLSI System Design & WMC) under R18-regulation

(Chairman-BOS)

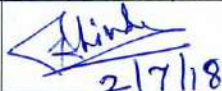


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Department of Electronics & Communication Engineering

Minutes of the meeting of the Board of Studies held on **02-07-2018** at **10:30am**.

The following members were present:

| SL.No | Members Present | Designation | Signature |
|-------|---|-------------------------|--|
| 1. | Mr. M. Shashidhar Assoc. Prof, Head, ECE Dept, VCE, Warangal | Chairman |  2/7/18 |
| 2. | Prof. M. AshaRani , ECE. Dept. | JNTUH Nominee |  02/7/18 |
| 3. | Dr. T. Kishore Kumar, Professor, ECE Dept. NIT, Warangal | Subject Expert |  2/7 |
| 4. | Prof. P. Prasad Rao VEC, Principal, Warangal | Subject Expert |  2/7/18 |
| 5. | Mr. P. Rohit, CEO, Suhrud Applab Private limited, Warangal | Industry Representative | |
| 6. | Mr. N. Kiran, JTO BSNL | Postgraduate Alumni | |
| 7. | Mr. K. Srinath, Jr Engg, NPDCL | Postgraduate Alumni | |
| 8. | Dr. Nishu Gupta, Asst. Prof, ECE Dept, VCE, Warangal | Member |  02/7/18 |
| 9. | Dr. Jitesh Ramdas Shinde, Asst. Prof, ECE Dept, VCE, Warangal | Member |  2/7/18 |

The following decisions are taken:

1. Approved the course structure for B. Tech. I,II, III & IV Years under R18 regulation.
2. Approved the syllabi of B.Tech. (R18-regulation) for I-Year I and II Semesters.
3. Resolved to follow previous regulation(R15) for PG Program.


(Chairman-BOS)

VAAGDEVI COLLEGE OF ENGINEERING

Autonomous
Bollikunta, Warangal

B.TECH. ELECTRONICS & COMMUNICATION ENGINEERING

COURSE STRUCTURE







(R18 Regulations applicable for the batches admitted from Academic Year 2018-19)

I SEMESTER (First Year)

| S.No. | Subject code | Subject | L | T | P | Credits |
|----------------------|--------------|---|---|---|---|-----------|
| 1 | B18MA01 | Mathematics-I (Linear Algebra & Calculus) | 3 | 1 | 0 | 4 |
| 2 | B18CS01 | Programming for Problem Solving | 4 | 0 | 0 | 4 |
| 3 | B18PH01 | Applied Physics | 4 | 0 | 0 | 4 |
| 4 | B18EN01 | English | 2 | 0 | 0 | 2 |
| 5 | B18PH02 | Physics Lab (Applied physics lab) | 0 | 0 | 3 | 1.5 |
| 6 | B18ME02 | Engineering Workshop & IT Workshop | 0 | 0 | 3 | 1.5 |
| 7 | B18CS02 | Programming for Problem Solving Lab | 0 | 0 | 2 | 1 |
| 8 | B18MC01 | National Service Scheme | 0 | 0 | 2 | 0 |
| Total Credits | | | | | | 18 |

II SEMESTER (First Year)

| S.No. | Subject code | Subject | L | T | P | Credits |
|----------------------|--------------|---|---|---|---|-----------|
| 1 | B18MA02 | Mathematics-II (Differential Equations & Vector Calculus) | 3 | 1 | 0 | 4 |
| 2 | B18CH01 | Engineering Chemistry | 3 | 1 | 0 | 4 |
| 3 | B18ME01 | Engineering Graphics | 2 | 0 | 2 | 3 |
| 4 | B18EE46 | Electrical circuits | 3 | 0 | 0 | 3 |
| 5 | B18EC01 | Electronic Devices and Circuits | 3 | 0 | 0 | 3 |
| 6 | B18EC02 | Electronic Devices and Circuits Lab | 0 | 0 | 2 | 1 |
| 7 | B18EN02 | English language & Communication Skills Lab | 0 | 0 | 2 | 1 |
| 8 | B18MC02 | Environmental Studies | 0 | 0 | 2 | 0 |
| Total Credits | | | | | | 19 |

- 1)  (M. Shashidhar)
- 2)  (M. Asha Rani)
- 3)  (DR. T. KISHORE KUMAR)
- 4)  (Dr. P. Prasad Rao)
- 5)  (Dr. Nikhil Gupta)
- 6)  (Dr. J.R. Shinde)

VAAGDEVI COLLEGE OF ENGINEERING

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B.TECH. ELECTRONICS & COMMUNICATION ENGINEERING

COURSE STRUCTURE







(R18 Regulations applicable for the batches admitted from Academic Year 2018-19)

III SEMESTER (Second Year)

| S.No. | Subject code | Subject | L | T | P | Credits |
|-------|--------------|--------------------------------------|---|---|---|-----------|
| 1 | | Complex Variable & Numerical Methods | 3 | 1 | 0 | 4 |
| 2 | | Signals and systems | 3 | 1 | 0 | 4 |
| 3 | | Electronic Circuits Analysis | 3 | 1 | 0 | 4 |
| 4 | | Switching Theory and Logic Design | 3 | 0 | 0 | 3 |
| 5 | | Electrical Technology | 3 | 0 | 0 | 3 |
| 6 | | Electronic Circuits Analysis Lab | 0 | 0 | 2 | 1 |
| 7 | | Simulation Lab | 0 | 0 | 2 | 1 |
| 8 | | Python Scripting Language | 0 | 0 | 2 | 1 |
| | | Total Credits | | | | 21 |

IV SEMESTER (Second Year)

| S.No. | Subject code | Subject | L | T | P | Credits |
|-------|--------------|--|---|---|---|-----------|
| 1 | | Pulse and Digital Circuits | 3 | 1 | 0 | 4 |
| 2 | | Electromagnetic Theory and Transmission Lines. | 3 | 1 | 0 | 4 |
| 3 | | Analog Communications & Digital Communications | 3 | 1 | 0 | 4 |
| 4 | | Probability Theory and Stochastic Process | 3 | 0 | 0 | 3 |
| 5 | | Computer Organization | 3 | 0 | 0 | 3 |
| 6 | | Pulse and digital circuits Lab | 0 | 0 | 2 | 1 |
| 7 | | Electrical Technology Lab | 0 | 0 | 2 | 1 |
| 8 | | Analog Communications & Digital Communications lab | 0 | 0 | 2 | 1 |
| | | Total Credits | | | | 21 |

- 1)  (M. Shashidhar)
- 2)  (M. Asharawi)
- 3)  (DR. T. KISHORE KUMAR)
- 4)  (Dr. P. Prasad Rao)
- 5)  (Dr. Nishu Gupta)
- 6)  (Dr. J. R. Shinde)

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Autonomous
Bollikunta, Warangal

B.TECH. ELECTRONICS & COMMUNICATION ENGINEERING

COURSE STRUCTURE

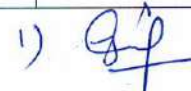
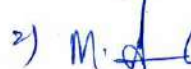




(R18 Regulations applicable for the batches admitted from Academic Year 2018-19)

V SEMESTER (Third Year)

| S.No. | Subject code | Subject | L | T | P | Credits |
|----------------------|--------------|---|---|---|---|-----------|
| 1 | | Linear & Digital IC Applications | 3 | 1 | 0 | 4 |
| 2 | | Digital Signal Processing | 3 | 0 | 0 | 3 |
| 3 | | Computer Networks | 3 | 0 | 0 | 3 |
| 4 | | Professional Elective-I Control Systems Telecommunication Switching Systems & Networks OOPS Through JAVA | 3 | 0 | 0 | 3 |
| 5 | | Managerial Economics & Financial Analysis | 3 | 0 | 0 | 3 |
| 6 | | LDIC Lab | 0 | 0 | 3 | 1.5 |
| 7 | | Digital Signal Processing Lab | 0 | 0 | 2 | 1 |
| 8 | | Computer Networks Lab | 0 | 0 | 3 | 1.5 |
| Total Credits | | | | | | 20 |

VI SEMESTER (Third Year)

| S.No. | Subject code | Subject | L | T | P | Credits |
|----------------------|--------------|---|---|---|---|-----------|
| 1 | | Microprocessors & Microcontrollers | 3 | 1 | 0 | 4 |
| 2 | | VLSI Design | 3 | 0 | 0 | 3 |
| 3 | | Antennas & Wave Propagation | 3 | 1 | 0 | 4 |
| 4 | | Professional Elective-II Bio Medical Instrumentation Data Communication Networks Digital Image Processing | 3 | 0 | 0 | 3 |
| 5 | | Professional Elective-III Radar Systems Digital Signal Processor & Architecture Real Time Operating Systems | 3 | 0 | 0 | 3 |
| 6 | | VLSI & e-CAD Lab | 0 | 0 | 2 | 1 |
| 7 | | Microprocessors & Microcontrollers Lab | 0 | 0 | 2 | 1 |
| 8 | | Advanced English Communication skills lab | 0 | 0 | 2 | 1 |
| Total Credits | | | | | | 20 |

- 1)  (M. Shashidhar)
- 2)  (M. Asharani)
- 3)  (DR. T. KULTORE KUMAR)
- 4)  (Dr. P. Prasad Rao)
- 5)  (Dr. Nishu Gupta)
- 6)  (Dr. J. R. Shinde)

VAAGDEVI COLLEGE OF ENGINEERING

Autonomous
Bollikunta, Warangal

B.TECH. ELECTRONICS & COMMUNICATION ENGINEERING

COURSE STRUCTURE


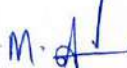
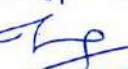



(R18 Regulations applicable for the batches admitted from Academic Year 2018-19)

VII SEMESTER (Fourth Year)

| S.No. | Subject code | Subject | L | T | P | Credits |
|-------|--------------|---|---|---|---|-----------|
| 1 | | Microwave Engineering | 3 | 0 | 0 | 3 |
| 2 | | Embedded Systems Design | 3 | 0 | 0 | 3 |
| 3 | | Professional Elective-IV Cellular Mobile Communication FPGA Architecture & Applications Artificial Intelligence | 3 | 0 | 0 | 3 |
| 4 | | Professional Elective-V Information Theory & Coding Satellite Communication Speech processing | 3 | 0 | 0 | 3 |
| 5 | | Open Elective – I | 3 | 0 | 0 | 3 |
| 6 | | Microwave Engineering Lab | 0 | 0 | 2 | 1 |
| 7 | | Embedded Systems Design Lab | 0 | 0 | 2 | 1 |
| 8 | | Mini Project and Internship | 0 | 0 | 0 | 2 |
| 9 | | Project Stage – I phase – I af | 0 | 0 | 8 | 4 |
| | | Total Credits | | | | 23 |

VIII SEMESTER (Fourth Year)

| S.No. | Subject code | Subject | L | T | P | Credits |
|-------|--------------|--|---|---|----|-----------|
| 1 | | Professional Elective-VI Fiber Optical Communications Low power VLSI Design Internet of Things | 3 | 0 | 0 | 3 |
| 2 | | Open Elective – II | 3 | 0 | 0 | 3 |
| 3 | | Open Elective – III | 3 | 0 | 0 | 3 |
| 4 | | Technical Seminar af | 0 | 0 | 2 | 1 |
| 5 | | Project Stage – II phase – II af | 0 | 0 | 16 | 8 |
| | | Total Credits | | | | 18 |

- 1)  (M. Shashidhar)
- 2)  (M. Asha Rani)
- 3)  (DR. T. KISHORE KUMAR)
- 4)  (Dr. P. Prasad Rao)
- 5)  (Dr. Nishu Gupta)
- 6)  (Dr. J. R. Shinde)

VAAGDEVI COLLEGE OF ENGINEERING

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Bollikunta, Warangal






B.TECH. ELECTRONICS & COMMUNICATION ENGINEERING

COURSE STRUCTURE

(R18 Regulations applicable for the batches admitted from Academic Year 2018-19)

List Of Open Electives

1. DBMS
2. Power Plant Engineering
3. Disaster Management
4. Cloud Computing
5. Entrepreneurship Development
6. Air Pollution Control
7. Robotics
8. Power Semi Conductor Drives
9. Industrial Electronics
10. Intellectual Property Rights
11. Machines Learning

- 1)  (M. Shachidhan)
- 2) M. A. Rai (M. AshaRani)
- 3)  (DR. T. KISHORE KUMAR)
- 4)  (Dr. P. Prasad Rao)
- 5)  (Dr. Nishu Gupta)
- 6)  (Dr. J. A. Shinde)

VAAGDEVI COLLEGE OF ENGINEERING

Autonomous
Bollikunta, Warangal

M.TECH. (VLSI System Design)

COURSE STRUCTURE


(R18 Regulations applicable for the batches admitted from Academic Year 2018-19 onwards)


I Semester (First Year)

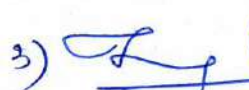
| S.No. | Subject code | Subject | L | T | P | Credits |
|----------------------|-------------------------------|--|---|---|---|-----------|
| 1 | M18VL01 | CMOS Digital Integrated Circuit Design | 3 | 0 | 0 | 3 |
| 2 | M18VL02 | CMOS Analog Integrated Circuit Design | 3 | 0 | 0 | 3 |
| 3 | M18VL03 M18VL04 M18VL05 | Program Elective-I Digital System Design using HDL VLSI Signal Processing VLSI Technology | 3 | 0 | 0 | 3 |
| 4 | M18VL06 M18VL07 M18VL08 | Program Elective-II Algorithms For VLSI Design Automation Embedded System Design Device Modeling | 3 | 0 | 0 | 3 |
| 6 | M18AC01 | English For Research Paper Writing | 2 | 0 | 0 | 0 |
| 7 | M18MC01 | Research Methodology | 2 | 0 | 0 | 2 |
| 8 | M18VL09 | HDL Programming Laboratory | 0 | 0 | 4 | 2 |
| 9 | M18VL10 | Digital IC Design Laboratory | 0 | 0 | 4 | 2 |
| Total Credits | | | | | | 18 |

II Semester (First Year)

| S.No. | Subject code | Subject | L | T | P | Credits |
|----------------------|-------------------------------|---|---|---|---|-----------|
| 1 | M18VL11 | CMOS Mixed Signal Circuit Design | 3 | 0 | 0 | 3 |
| 2 | M18VL12 | VLSI Design Verification and Testing | 3 | 0 | 0 | 3 |
| 3 | M18VL13 M18VL14 M18VL15 | Program Elective-III Low Power VLSI Design Optimization Technique In VLSI Design High Speed VLSI Design | 3 | 0 | 0 | 3 |
| 4 | M18VL16 M18VL17 M18VL18 | Program Elective-IV ASIC Design System On Chip Architecture Semiconductor Memory Design & Testing | 3 | 0 | 0 | 3 |
| 5 | M18AC02 | Stress Management | 2 | 0 | 0 | 0 |
| 6 | M18VL19 | Analog IC Design Laboratory | 0 | 0 | 4 | 2 |
| | M18VL20 | Mixed Signal VLSI Laboratory | 0 | 0 | 4 | 2 |
| 7 | M18VL21 | Mini Project/ Internship | 2 | 0 | 0 | 2 |
| Total Credits | | | | | | 18 |

1)  M. Sheshidhar

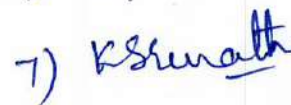
2)  (M. ASHA RANI)


3)  (Dr. T. Kishore Kumar)


4)  (Dr. P. Prasad Rao)

5) 

6) 

7)  K. Srinath

8)  Dr. Nishu Gupta

9)  Dr. J. R. Shinde

VAAGDEVI COLLEGE OF ENGINEERING

Autonomous
Bollikunta, Warangal

M.TECH. (VLSI System Design)

COURSE STRUCTURE

(R18 Regulations applicable for the batches admitted from Academic Year 2018-19 onwards)

III SEMESTER (Second Year)

| S.No. | Subject code | Subject | L | T | P | Credits |
|----------------------|--------------|---|---|---|----|-----------|
| 1 | M18VL22 | Program Elective-V High Speed VLSI Architectures for DSP Applications | 3 | 0 | 0 | 3 |
| | M18VL23 | Nano materials & Nano Technology | | | | |
| | M18VL24 | RF Circuit Design | | | | |
| 2 | M18CS12 | Open Elective Soft Computing Techniques | 3 | 0 | 0 | 3 |
| | M18MA02 | Graph Theory & Optimization Techniques | | | | |
| | M18CE27 | Waste Management | | | | |
| 3 | M18VL25 | Dissertation Phase – I | 0 | 0 | 20 | 10 |
| Total Credits | | | | | | 16 |

IV SEMESTER (Second Year)

| S.No. | Subject code | Subject | L | T | P | Credits |
|----------------------|--------------|-------------------------|---|---|----|-----------|
| 1 | M18VL26 | Dissertation Phase – II | 0 | 0 | 32 | 16 |
| Total Credits | | | | | | 16 |

1) M. Seshidhar

2) M. A. Bee

3) Thy

4) Di

5) Dej

6) NH

7) K. Srinath

8) Dr. Nishu Gupta

9) Dr. J. R. Shinde

VAAGDEVI COLLEGE OF ENGINEERING

Autonomous
Bollikunta, Warangal

M.Tech (Wireless and Mobile Communications)

COURSE STRUCTURE






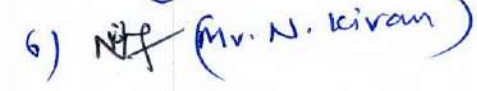



(R18 Regulations applicable for the batches admitted from Academic Year 2018-19 onwards)

I Semester (First Year)

| S.No. | Subject code | Subject | L | T | P | Credits |
|----------------------|-------------------------------|--|---|---|---|-----------|
| 1. | M18WM01 | Advanced Data Communications | 3 | 0 | 0 | 3 |
| 2. | M18WM02 | Coding Theory and Techniques | 3 | 0 | 0 | 3 |
| 3. | M18WM03 M18WM04 M18WM05 | Program Elective-I Spread Spectrum Communication Detection & Estimation Theory Stochastic Process & Time Domain Analysis | 3 | 0 | 0 | 3 |
| 4. | M18WM06 M18WM07 M18WM08 | Program Elective-II Voice Over Internet Protocol Internetworking GPS and Applications | 3 | 0 | 0 | 3 |
| 5. | M18AC01 | English For Research Paper Writing | 2 | 0 | 0 | 0 |
| 6. | M18MC01 | Research Methodology | 2 | 0 | 0 | 2 |
| 7. | M18WM09 | Advanced Communications Laboratory | 0 | 0 | 4 | 2 |
| 8. | M18WM10 | Wireless Communications Network Laboratory Laboratory | 0 | 0 | 4 | 2 |
| Total Credits | | | | | | 18 |

II Semester (First Year)

| S.No. | Subject code | Subject | L | T | P | Credits |
|----------------------|-------------------------------|--|---|---|---|-----------|
| 1. | M18WM11 | Advanced Digital Signal Processing | 3 | 0 | 0 | 3 |
| 2. | M18WM12 | Wireless Communications | 3 | 0 | 0 | 3 |
| 3. | M18WM13 M18WM14 M18WM15 | Program Elective-III Advanced Communications and Networks Embedded System Design Optical Communications Technology | 3 | 0 | 0 | 3 |
| 4. | M18WM16 M18WM17 M18WM18 | Program Elective-IV Wireless MIMO Communication Wireless LANs and PANs Software Defined Radio | 3 | 0 | 0 | 3 |
| 5. | M18AC02 | Stress Management | 2 | 0 | 0 | 0 |
| 6. | M18WM19 | Formatting and Analysis Laboratory | 0 | 0 | 4 | 2 |
| 7. | M18WM20 | Simulation Laboratory | 0 | 0 | 4 | 2 |
| 8. | M18WM21 | Mini Project/ Internship | 2 | 0 | 0 | 2 |
| Total Credits | | | | | | 18 |

- | | |
|---|--|
| <p>1)  M. Shashidhar</p> <p>2)  M. A. Lei (M. Asha Ravi)</p> <p>3)  (Dr. T. Kishore Kumar)</p> <p>4) </p> | <p>5) </p> <p>6)  (Mr. N. Kiran)</p> <p>7) </p> <p>8)  Dr. Nishu Gupta</p> <p>9)  Dr. J. R. Shinde</p> |
|---|--|

VAAGDEVI COLLEGE OF ENGINEERING

Autonomous
Bollikunta, Warangal

M.Tech (Wireless and Mobile Communications)

COURSE STRUCTURE




(R18 Regulations applicable for the batches admitted from Academic Year 2018-19 onwards)


III SEMESTER (Second Year)

| S.No. | Subject code | Subject | L | T | P | Credits |
|----------------------|-------------------------------|--|---|---|----|-----------|
| 1 | M18WM22 M18WM23 M18WM24 | Program Elective-V 4G & 5G Technologies Mobile Computing Technologies Adhoc and Wireless Sensor Networks | 3 | 0 | 0 | 3 |
| 2 | M18CS05 M18MA01 M18CE27 | Open Elective Scripting Languages Advanced Optimization Techniques Waste Management | 3 | 0 | 0 | 3 |
| 3 | M18WM25 | Dissertation Phase – I | 0 | 0 | 20 | 10 |
| Total Credits | | | | | | 16 |

IV SEMESTER (Second Year)

| S.No. | Subject code | Subject | L | T | P | Credits |
|----------------------|--------------|-------------------------|---|---|----|-----------|
| 1 | M18WM26 | Dissertation Phase – II | 0 | 0 | 32 | 16 |
| Total Credits | | | | | | 16 |

- 1) Prof M. Shashidhar
- 2) M. A. Sai (M. Asha Lakshmi)
- 3) 
- 4) 
- 5) Prof
- 6) 

- 7) K. K. K. K.
- 8) Prof. Dr. Nishu Gupta
- 9)  Dr. J. R. Ginde