

Autonomous

Bollikunta, Khila Warangal (Mandal), Warangal Urban-506 005 (T.S), www.vaagdevi.edu.in DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

### <u>Course Outcomes for M.Tech – VLSI SYSTEM DESIGN (R20)</u> <u>for the academic year 2020-2021 onwards</u>

Course	Semester	CMOS Digital Integrated Circuit	L: 3 T: 0 P: 0 C: 3	
Outcome	I Sem	Design (M20VL01)		
After the co	mpletion of this c	ourse, the students should be able to		
1	Define the basic of	CMOS technology.		
2	Relate, compare, in implementation, and	nterpret and make the use of the best CMOS alysis & design of Combinational& Sequential 1	S design techniques for MOS logic circuits.	
3	Know & tell different types of memories and compare performance evaluation of each memory modules so they can be able to think & justify how to improve performance by taking different structures			
4	Define, simplify & justify which dynamic logic circuit can be used investigate CMOS circuits.			
5	Recommend variou constraints requirem	s CMOS techniques and also other device technent.	nologies based on circuit	
Course	Semester	<b>CMOS Analog Integrated Circuit</b>	L: 3 T: 0 P: 0 C: 3	
Outcome	I Sem	Design (M20VL02)		
After the co	ompletion of this course, the students should be able to			
1	Define the parameters of MOS Devices & can predict the performance or behavior of Analog VLSI circuit.			
2	Analyze & characterize analog devices and systems to achieve performance specifications.			
3	Understand the different topologies involved in the CMOS amplifier design.			
4	Understand design issues & measurement techniques related to CMOS operational amplifier design.			
5	Design & analyze Specifications.	the comparator for different topologies to achie	ve performance	
Course	Semester	(Program Elective-I) Digital System	L: 3 T: 0 P: 0 C: 3	
Outcome	I Sem	Design using HDL (M20VL03)		
After the completion of this course, the students should be able to				
1	Understand the basic concepts of Verilog HDL, digital system design flow, timing, and synthesis and FPGA implementation issues.			
2	Understand the basics of MOS transistors required for MOS based circuit & layout design.			
3	Know the different design technique for CMOS Combinational Circuit Design & able to select suitable design technique for given performance specification.			
4	Get an idea of the to select suitable d	different design technique for CMOS Sequenti esign technique for given performance specifica	al Circuit Design & able	
5	Understand the design flow from simulation to synthesizable / implementation level for VLSI based system design.			
Course	Semester	(Program Elective-I) VLSI Signal	L: 3 T: 0 P: 0 C: 3	
Outcome	I Sem	Processing (M20VL04)		



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After the co	mpletion of this c	ourse, the students should be able to		
1	Understand the overview of DSP concepts.			
2	Apply the concepts of iteration bound, pipelining& parallel processing for FIR filter design.			
3	Understand techni structures.	ques of fast convolution & algorithmic streng	th reduction in the filter	
4	Perform pipelining speed & low powe	g & parallel processing on recursive filter str r.	uctures to achieve high	
5	Use of proper tech	niques for parallel processing design for scaling	and round off noise.	
Course	Semester	(Program Elective-I) VLSI Technology	L: 3 T: 0 P: 0 C: 3	
Outcome	I Sem	(M20VL05)		
After the co	mpletion of this c	ourse, the students should be able to		
1	Understand the dif	ferent MOS technologies.		
2	Appreciate the var	ious techniques involved in the VLSI fabrication	n process.	
3	Analyze the concepts, transistor structures, interconnects & design rules related to layout design in VLSI.			
4	Understand the dif	ferent doping & diffusion mechanism.		
5	Understand the m packaging of VLS	uances of design rules, scaling, transistors, I devices.	resistors, capacitors &	
12	Semester	(Program Elective-II) Algorithms For	L: 3 T: 0 P: 0 C: 3	
	I Sem	VLSI Design Automation (M20VL06)		
After the co	mpletion of this c	ourse, the students should be able to		
1	Understand the preliminaries required for VLSI system design.			
2	Apply the general purpose methods for combinational optimization.			
3	Understand the co	oncept of Layout Compaction, Placement, Flo	oor planning& Routing,	
	modeling & simul	ation involved in VLSI system design.		
4	Analyze the conce	pt related to synthesis & verification in VLSI sy	stem design.	
5	Analyze the design	n cycle of for FPGA and partitioning-routing co	ncepts related to it.	
6	Explain the algorithms for partitioning, floor planning, placement and routing the MCM modules.			
Course	Semester	(Program Elective-II) Embedded	L: 3 T: 0 P: 0 C: 3	
Outcome	I Sem	System Design (M20VL07)		
After the co	mpletion of this c	ourse, the students should be able to		
1	Know the Basic C	oncept of Embedded Systems.		
2	Understand the core of typical embedded system.			
3	Know the embedded firmware.			
4	Get introduced to 1	RTOS based Embedded system design & related	d mechanism.	
5	Appreciate the m embedded.	nethods for task communication for the dev	velopment of a typical	
Course	Semester	(Program Elective-II) Device Modeling	L: 3 T: 0 P: 0 C: 3	
Outcome	I Sem	(M20VL08)		
After the co	mpletion of this c	ourse, the students should be able to		



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1	Understand the physics of and design elements of silicon MOSFETs.			
2	Understand & study the physics behind the operation of integrated diodes & integrated			
	bipolar transistor.			
3	Analyze& study the physics behind the operation of integrated diodes & integrated bipolar			
	transistor.			
4	Understand the VI	SI fabrication techniques.		
5	To design circuits	using Hetero Junction Devices with physical in	sight of their functional.	
Course	Semester	English For Research Paper Writing	L: 2 T: 0 P: 0 C: 0	
Outcome	I Sem	( <b>M20AC01</b> )		
After the co	mpletion of this c	ourse, the students should be able to		
1	Develop the conte	ent, structure and format of writing a research	paper.	
2	Understand the re	search methodology in research paper writing	5.	
3	Analyze and prac	tice writing a Research Paper.		
4	Know how to & v	where to get published the research work.		
Course	Semester	Research Methodology (M20MC01)	L: 2 T: 0 P: 0 C: 2	
Outcome	I Sem			
After the co	After the completion of this course, the students should be able to			
1	Appreciate the flow	w of research methodologies in the research wo	rk.	
2	Design Important	Concepts Related to Research Design.		
3	Learn better report	writing skills and Patenting.		
4	To write a Researc	h Proposal and Research Report & Research G	rant Proposal.	
5	Understand the im	portance of Intellectual Property.	•	
Course	Semester	HDL Programming Laboratory	L: 0 T: 0 P: 4 C: 2	
Outcome	I Sem	(M20VL09)		
1	Apply the knowled	lge in Simulation and Synthesis of Digital Circu	uits.	
2	DesignVariousCon	nbinationalandSequentialcircuitsusingVerilogH	DL&HDL.	
3	Explain the System	n Modeling with Tasks and Functions.		
4	Design of digital c	ircuits using FPGA/CPLD boards.		
Course	Semester	Digital IC Design Laboratory	L: 0 T: 0 P: 4 C: 2	
Outcome	I Sem	(M20VL10)		
After the completion of this course, the students should be able to				
1	Design CMOS inv	Design CMOS inverters, logic circuits and transmission gates to specifications.		
2	Design latches and flip-flops as the basic circuit for Random-Access- Memory (RAM) and			
	Read-Only-Memory (ROM) cells.			
3	Understand the Design of Bi-CMOS Inverter, logic circuits.			
4	Design post Layou	Design post Layout of Different logic circuits.		
Course	Semester	CMOS Mixed Signal Circuit Design	L: 3 T: 0 P: 0 C: 3	
Outcome	II Sem	(M20VL11)		
After the co	mpletion of this c	ourse, the students should be able to		
1	Build mixed signa	l circuits like DAC, ADC, PLL etc &Gain know	wledge on filter design in	
1	mixed signal mode & To acquire knowledge on design different architectures in mixed			



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	signal mode.		
2	Analyze digital test and linear test engineers to the mixed signal world by teaching the		
	basics of analog and mixed signal test methods. Sampling Theory, Frequency Domain		
	Testing, and Digita	al Signal Processing.	
3	Apply these fundamental concepts to different test methods and data validation for mixed		
	signal parameters together with debugging, noise reduction and device interface		
	techniques.		
4	Deal with the the	ory and design skills of CMOS op-amps, vo	oltage reference circuits,
	switched capacitor circuits, sample-and- hold circuits, and A/D & D/A converters used in		
	modern communic	ation systems and consumer electronic products	s.
5	Design of core mi	xed-signal IC blocks: comparators and data co	onverters & System level
	design flow: top-d	own and bottom-up design methodologies.	
Course	Semester	VLSI Design Verification and Testing	L: 3 T: 0 P: 0 C: 3
0	TLC	(M20VL12)	
Outcome	II Sem	()	
After the co	mpletion of this c	ourse, the students should be able to	
1	Understand the ne	eed for testing in VI SI & different testing issu	165
2	Gain the knowle	edge of testing and verification in VI SI	design process ATPG
2	concepts for com	vige of testing and verification in vest v	uesign process, Arro
3	Apply knowledge of testability measures for testing of digital systems		
3	Apply knowledge of testaonity measures for testing of digital systems.		
4	Apply knowledge of test-pattern generation & Design for testability techniques for		
5	testing of digital systems.		
5	Understanding bo	undary scan standards & testing techniques to	Dr CIVIOS IC S.
Course	Semester	(Program Elective-III) Low Power	L: 3 1: 0 P: 0 C: 3
Outcome	II Sem	VLSI Design (M20VL13)	
Outcome After the co	II Sem mpletion of this c	VLSI Design (M20VL13) ourse, the students should be able to	
Outcome After the con	II Sem mpletion of this c Understand the m	<b>VLSI Design (M20VL13)</b> <b>ourse, the students should be able to</b> eed for low power circuit design & sources	of power dissipation in
Outcome After the con 1	II Sem mpletion of this c Understand the n VLSI system.	VLSI Design (M20VL13) ourse, the students should be able to eed for low power circuit design & sources	of power dissipation in
Outcome After the con 1	II Sem mpletion of this c Understand the n VLSI system.	VLSI Design (M20VL13) ourse, the students should be able to eed for low power circuit design & sources	of power dissipation in
Outcome After the con 1 2 3	II Sem mpletion of this c Understand the m VLSI system. Appreciate the co	VLSI Design (M20VL13) ourse, the students should be able to eed for low power circuit design & sources ncept of Low-Power Design Approaches in V	of power dissipation in /LSI system design.
Outcome After the con 1 2 3 4	II Sem mpletion of this c Understand the n VLSI system. Appreciate the co Design low voltag	VLSI Design (M20VL13) ourse, the students should be able to eed for low power circuit design & sources ncept of Low-Power Design Approaches in V ge low power adders for given performance sp	of power dissipation in /LSI system design. pecification.
Outcome After the con 1 2 3 4	II Sem mpletion of this c Understand the n VLSI system. Appreciate the co Design low voltag Optimize the po	VLSI Design (M20VL13) ourse, the students should be able to eed for low power circuit design & sources ncept of Low-Power Design Approaches in V ge low power adders for given performance sp wer of multiplier using different strategies	of power dissipation in /LSI system design. pecification. at different levels of
Outcome After the con 1 2 3 4 5	II Sem mpletion of this c Understand the m VLSI system. Appreciate the co Design low voltag Optimize the po design.	VLSI Design (M20VL13) ourse, the students should be able to eed for low power circuit design & sources ncept of Low-Power Design Approaches in V ge low power adders for given performance sp wer of multiplier using different strategies	of power dissipation in /LSI system design. pecification. at different levels of
Outcome After the con 1 2 3 4 5 Course	II Sem mpletion of this c Understand the m VLSI system. Appreciate the co Design low voltag Optimize the po design. Design low-powe	VLSI Design (M20VL13) ourse, the students should be able to eed for low power circuit design & sources ncept of Low-Power Design Approaches in V ge low power adders for given performance sp wer of multiplier using different strategies r CMOS memories using various strategies at	of power dissipation in /LSI system design. pecification. at different levels of different design level.
Outcome After the con 1 2 3 4 5 Course	II Sem mpletion of this c Understand the n VLSI system. Appreciate the co Design low voltag Optimize the po design. Design low-powe Semester	VLSI Design (M20VL13) ourse, the students should be able to eed for low power circuit design & sources ncept of Low-Power Design Approaches in V ge low power adders for given performance sp wer of multiplier using different strategies r CMOS memories using various strategies at (Program Elective-III) Optimization	of power dissipation in CLSI system design. Decification. at different levels of c different design level. L: 3 T: 0 P: 0 C: 3
Outcome After the con 1 2 3 4 5 Course Outcome	II Sem mpletion of this c Understand the m VLSI system. Appreciate the co Design low voltag Optimize the po design. Design low-powe Semester II Sem	VLSI Design (M20VL13) ourse, the students should be able to eed for low power circuit design & sources ncept of Low-Power Design Approaches in V ge low power adders for given performance sp wer of multiplier using different strategies r CMOS memories using various strategies at (Program Elective-III) Optimization Technique In VLSI Design	of power dissipation in /LSI system design. Decification. at different levels of different design level. L: 3 T: 0 P: 0 C: 3
Outcome After the con 1 2 3 4 5 Course Outcome	II Sem mpletion of this c Understand the n VLSI system. Appreciate the co Design low voltag Optimize the po design. Design low-powe Semester II Sem	VLSI Design (M20VL13) ourse, the students should be able to eed for low power circuit design & sources ncept of Low-Power Design Approaches in V ge low power adders for given performance sp wer of multiplier using different strategies r CMOS memories using various strategies at (Program Elective-III) Optimization Technique In VLSI Design (M20VL14)	of power dissipation in (LSI system design. becification. at different levels of c different design level. L: 3 T: 0 P: 0 C: 3
Outcome After the con 1 2 3 4 5 Course Outcome After the con	II Sem mpletion of this c Understand the ne VLSI system. Appreciate the co Design low voltag Optimize the po design. Design low-powe Semester II Sem mpletion of this c	VLSI Design (M20VL13) ourse, the students should be able to eed for low power circuit design & sources ncept of Low-Power Design Approaches in V ge low power adders for given performance sp wer of multiplier using different strategies r CMOS memories using various strategies at (Program Elective-III) Optimization Technique In VLSI Design (M20VL14) ourse, the students should be able to	of power dissipation in <u>'LSI system design.</u> <u>becification.</u> at different levels of <u>c different design level.</u> L: 3 T: 0 P: 0 C: 3
Outcome After the con 1 2 3 4 5 Course Outcome After the con 1	II Sem mpletion of this c Understand the m VLSI system. Appreciate the co Design low voltag Optimize the por design. Design low-powe Semester II Sem mpletion of this c Gain knowledge	VLSI Design (M20VL13) ourse, the students should be able to eed for low power circuit design & sources ncept of Low-Power Design Approaches in V ge low power adders for given performance sp wer of multiplier using different strategies r CMOS memories using various strategies at (Program Elective-III) Optimization Technique In VLSI Design (M20VL14) ourse, the students should be able to on Optimization techniques involved in VL	of power dissipation in <u>'LSI system design.</u> Decification. at different levels of different design level. L: 3 T: 0 P: 0 C: 3 SI circuits.
Outcome After the con 1 2 3 4 5 Course Outcome After the con 1 2	II Sem mpletion of this c Understand the m VLSI system. Appreciate the co Design low voltag Optimize the po design. Design low-powe Semester II Sem mpletion of this c Gain knowledge Analyze method	VLSI Design (M20VL13) ourse, the students should be able to eed for low power circuit design & sources ncept of Low-Power Design Approaches in V ge low power adders for given performance sp wer of multiplier using different strategies r CMOS memories using various strategies at (Program Elective-III) Optimization Technique In VLSI Design (M20VL14) ourse, the students should be able to on Optimization to engineering stude	of power dissipation in (LSI system design. becification. at different levels of different design level. L: 3 T: 0 P: 0 C: 3 SI circuits. ents. including linear
Outcome After the con 1 2 3 4 5 Course Outcome After the con 1 2 2 3 4 4 5 5 Course 0 1 2 3 4 5 5 Course Course 1 2 3 5 Course 1 2 5 Course Co	II Sem mpletion of this c Understand the m VLSI system. Appreciate the co Design low voltag Optimize the po design. Design low-powe Semester II Sem mpletion of this c Gain knowledge Analyze method programming no	VLSI Design (M20VL13) ourse, the students should be able to eed for low power circuit design & sources ncept of Low-Power Design Approaches in V ge low power adders for given performance sp wer of multiplier using different strategies r CMOS memories using various strategies at (Program Elective-III) Optimization Technique In VLSI Design (M20VL14) ourse, the students should be able to on Optimization techniques involved in VL ls of optimization to engineering stude onlinear programming, and heuristic method	of power dissipation in <u>'LSI system design.</u> pecification. at different levels of different design level. L: 3 T: 0 P: 0 C: 3 <u>SI circuits.</u> ents, including linear
Outcome After the con 1 2 3 4 5 Course Outcome After the con 1 2 3	II Sem mpletion of this c Understand the m VLSI system. Appreciate the co Design low voltag Optimize the por design. Design low-powe Semester II Sem mpletion of this c Gain knowledge Analyze method programming, no	VLSI Design (M20VL13) ourse, the students should be able to eed for low power circuit design & sources ncept of Low-Power Design Approaches in V ge low power adders for given performance sp wer of multiplier using different strategies r CMOS memories using various strategies at (Program Elective-III) Optimization Technique In VLSI Design (M20VL14) ourse, the students should be able to on Optimization techniques involved in VL ls of optimization to engineering stude onlinear programming, and heuristic method nce between theory numerical computation	of power dissipation in <u>'LSI system design.</u> <u>becification.</u> at different levels of <u>c different design level.</u> <u>L: 3 T: 0 P: 0 C: 3</u> <u>SI circuits.</u> <u>ents, including linear</u> <u>ls.</u> on problem setup for
Outcome After the con 1 2 3 4 5 Course Outcome After the con 1 2 3	II Sem mpletion of this c Understand the m VLSI system. Appreciate the co Design low voltag Optimize the po design. Design low-powe Semester II Sem mpletion of this c Gain knowledge Analyze method programming, no Understand bala solution by optim	VLSI Design (M20VL13) ourse, the students should be able to eed for low power circuit design & sources ncept of Low-Power Design Approaches in V ge low power adders for given performance sp wer of multiplier using different strategies r CMOS memories using various strategies at (Program Elective-III) Optimization Technique In VLSI Design (M20VL14) ourse, the students should be able to on Optimization to engineering stude pulinear programming, and heuristic method nce between theory, numerical computation	of power dissipation in (LSI system design. Decification. at different levels of different design level. L: 3 T: 0 P: 0 C: 3 SI circuits. ents, including linear ls. on, problem setup for pering systems
Outcome         After the control         1         2         3         4         5         Course         Outcome         1         2         3         4         5         Course         Outcome         1         2         3	II Sem mpletion of this c Understand the m VLSI system. Appreciate the co Design low voltag Optimize the po design. Design low-powe Semester II Sem mpletion of this c Gain knowledge Analyze method programming, no Understand bala solution by optim	VLSI Design (M20VL13) ourse, the students should be able to eed for low power circuit design & sources ncept of Low-Power Design Approaches in V ge low power adders for given performance sp wer of multiplier using different strategies r CMOS memories using various strategies at (Program Elective-III) Optimization Technique In VLSI Design (M20VL14) ourse, the students should be able to on Optimization techniques involved in VL ds of optimization to engineering stude onlinear programming, and heuristic method nce between theory, numerical computation ization software, and applications to engine	of power dissipation in /LSI system design. Decification. at different levels of different design level. L: 3 T: 0 P: 0 C: 3 SI circuits. ents, including linear ls. on, problem setup for pering systems. fficient conditions for
Outcome         After the control         1         2         3         4         5         Course         Outcome         After the control         1         2         3         4         5         Course         Outcome         3         4	II Sem mpletion of this c Understand the m VLSI system. Appreciate the co Design low voltag Optimize the po design. Design low-powe Semester II Sem mpletion of this c Gain knowledge Analyze method programming, no Understand bala solution by optim Studies General	VLSI Design (M20VL13) ourse, the students should be able to eed for low power circuit design & sources ncept of Low-Power Design Approaches in V ge low power adders for given performance sp wer of multiplier using different strategies r CMOS memories using various strategies at (Program Elective-III) Optimization Technique In VLSI Design (M20VL14) ourse, the students should be able to on Optimization techniques involved in VL ls of optimization to engineering stude onlinear programming, and heuristic method nce between theory, numerical computation ization software, and applications to engine optimization algorithm; necessary and su	of power dissipation in <u>'LSI system design.</u> <u>becification.</u> at different levels of <u>c different design level.</u> <u>L: 3 T: 0 P: 0 C: 3</u> <u>SI circuits.</u> ents, including linear <u>ls.</u> on, problem setup for <u>tering systems.</u> fficient conditions for
Outcome         After the control         1         2         3         4         5         Course         Outcome         After the control         1         2         3         4         5         Outcome         3         4         2         3         4	II Sem mpletion of this c Understand the m VLSI system. Appreciate the co Design low voltag Optimize the po design. Design low-powe Semester II Sem mpletion of this c Gain knowledge Analyze method programming, no Understand bala solution by optim Studies General optimality.	VLSI Design (M20VL13) ourse, the students should be able to eed for low power circuit design & sources ncept of Low-Power Design Approaches in V ge low power adders for given performance sp wer of multiplier using different strategies r CMOS memories using various strategies at (Program Elective-III) Optimization Technique In VLSI Design (M20VL14) ourse, the students should be able to on Optimization techniques involved in VL ls of optimization to engineering stude onlinear programming, and heuristic method nce between theory, numerical computation ization software, and applications to engine optimization algorithm; necessary and su	of power dissipation in <u>'LSI system design.</u> Decification. at different levels of different design level. <u>L: 3 T: 0 P: 0 C: 3</u> <u>SI circuits.</u> ents, including linear ls. on, problem setup for pering systems. fficient conditions for



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Course	Semester	(Program Elective-III) High Speed	L: 3 T: 0 P: 0 C: 3	
Outcome	II Sem	VLSI Design (M20VL15)		
After the co	mpletion of this course, the students should be able to			
1	Appreciate the different clocking logic styles in VLSI system design as per			
2	Understand circu	it design margining & design variability for V	LSI circuit.	
3	Appreciate the co	oncept of latching strategies to optimize the spo	eed of the system.	
4	Gainknowledgeo	ninterfacetechniquesinvolvedinhighspeedVLS	Icircuits.	
5	Analyze the cloo	cking styles in design to optimize the timing	issues to support high	
Course	Semester	(Program Elective-IV) ASIC Design	L: 3 T: 0 P: 0 C: 3	
Outcome	II Sem	(M20VL16)		
After the co	mpletion of this	course, the students should be able to		
1	To learn the fund	amentals of ASIC and its design methods.		
2	To gain knowledg	ge on programmable architectures for ASICs & p	hysical design of ASIC.	
3	Understand the programmable ASIC Logic Cells & selection of suitable ASIC Logic cells for design.			
4	Analyze ASIC flo	oor planning, placement and routing in VLSI Des	ign.	
5	Appreciate conce	pt of optimization algorithms in the design of an	efficient layout.	
Course	Semester	(Program Elective-IV) System On	L: 3 T: 0 P: 0 C: 3	
Outcome	II Sem	Chip Architecture (M20VL17)		
After the completion of this course, the students should be able to				
1	Apply the knowledge of SoC architecture & organization.			
2	Analyze various p	processor microarchitecture & design trade-off for	or SoC.	
3	Understand the memory design for SoC.			
4	Evaluate intercon	nect structure for different topologies.		
5	Design Soc based	Embedded system on FPGA.	<b>I</b> . <b>2T</b> . <b>0D</b> . <b>0C</b> . <b>2</b>	
Course	Semester	(Program Elective-IV) Semiconductor	L: 3 1: 0 P: 0 C: 3	
Outcome	II Sem	Memory Design & Testing (M20VL18)		
After the completion of this course, the students should be able to				
1	Know the design of MOS memories and the various precautionary methods to be used in their design.			
2	Learn overview of memory chip design, DRAM circuits, voltage generators, performance analysis and design issues of ultra-low voltage memory circuits			
3	Acquire knowledge about High-Performance Subsystem Memories & Analyze RAM and DRAM Design			
4	Demonstrate Ad	vanced Memory Technologies and High-der Gains knowledge on various testing methods of se	sity Memory Packing	
5	Get an overview	on reliability of semiconductors and their testing	enteonauctor memories.	
Course	Semester	Stress Management (M20AC02)	L: 2 T: 0 P: 0 C: 0	
Outcome	II Sem			



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After the co	mpletion of this c	course, the students should be able to		
1	Enhance of Physical strength and flexibility.			
2	Learn to relax and focus.			
3	Relieve physical a	nd mental tension.		
4	Improve work per	formance/ efficiency.		
Course	Semester	Analog IC Design Laboratory	L: 0 T: 0 P: 4 C: 2	
Outcome	II Sem	(M20VL19)		
After the co	mpletion of this c	course, the students should be able to		
1	Design Various Cl	haracteristics of MOS Logic.		
2	Design Various A	mplifier circuits using CMOS Logic.		
3	Design Various cit	rcuits using Different Logic Styles.		
4	Design Layout of	Different logic circuits.		
Course	Semester	Mixed Signal VLSI Laboratory	L: 0 T: 0 P: 4 C: 2	
Outcome	II Sem	(M20VL20)		
After the completion of this course, the students should be able to				
1	Design Various A	mplifier circuits using CMOS Logic.		
2	Design Various Complex circuits using Different Logic Styles.			
3	Design Layout of	Different logic circuits.		
4	Digital/analog circuits are to be designed and implemented using CAD tools.			
Course	Semester	Mini Project (M20VL21)	L: 0 T: 0 P: 4 C: 2	
Outcome	II Sem			
After the cor	npletion of this co	urse, the students should be able to		
1	Use fundamental knowledge and skills in engineering and apply it effectively on a project.			
2	UnderstandthePro	ductDevelopmentProcessincludingbudgetingthro	oughMiniProject.	
3	Plan for various ac	Plan for various activities of the Miniproject.		
4	Inculcate electronic hardware and software implementation skills.			
5	Manage any dispu	tes and conflicts within and outside individually	<i>.</i>	
6	Prepare a technical report based on the Miniproject.			
7	Deliver technical seminar based on the Mini Project work carried out.			
Course	Semester		L: 3 T: 0 P: 0 C: 3	
Outcome	III Sem	(Program Elective-V)		
		High Speed VLSI Architectures for		
		DSP Applications (M20VL22)		
After the cor	npletion of this co	urse, the students should be able to		
1	Apply the concept of unfolding for optimization of critical paths in the VLSI system design.			
2	Design Multiplier architectures in optimized way for given specification in VLSI Design.			
2	Design Multiplier	architectures in optimized way for given specifi	cation in vLSi Design.	
3	Design Multiplier Apply the redund used in digital sign	ant arithmetic for optimization of adder & m nal processing application.	ultiplier block generally	



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	performance of High Speed VLSI Design.			
5	Understand the low power VLSI DSP system.			
Course	Semester	(Program Elective-V)	L: 3 T: 0 P: 0 C: 3	
Outcome	III Sem	Nano materials & Nano Technology		
		(M20VL23)		
After the cor	mpletion of this	course, the students should be able to		
1	Understand the	limitations of the MOSFETs & potential of nanoe	lectronics.	
2	Show a deeper understanding of the relation between novel behavior of nanoelectronics devices and quantum behavior of the matter at the nano scale as well as the breakdown of received scaling wisdom			
3	Understand stru	ctures of carbon nanotubes & its applications.		
4	Appreciate the ounderstand the p	concept of molecular electronics in nanoscale fabr principle of spintronic.	ication technologies	
Course	Semester	(Program Elective-V)	L: 3 T: 0 P: 0 C: 3	
Outcome	III Sem	RF Circuit Design (M20VL24)		
After the con	npletion of this	course, the students should be able to		
1	Understand the	performance parameters / specifications of the RF	Circuits.	
2	Design & analy	ze the filter design.		
3	Understand & evaluate the performance of various specifications of high frequency amplifier design, Mixer, Oscillators & Power Amplifiers.			
4	Understand the source of nonlinearity, noise, process technology & its impact on the parameters of individual blocks of receiver & on receiver performance.			
5	Demonstrate the building blocks.	e tools & techniques to evaluate the performance	specifications of the RF	
Course	Semester	(Open Elective) Soft Computing	L: 3 T: 0 P: 0 C: 3	
Outcome	III Sem	Techniques (M20CS12)		
After the con	npletion of this	course, the students should be able to		
1	Understand the Fundamentals of Neural Networks & Feed Forward Networks.			
2	Design & analyze the Associative Memories & ART Neural Networks.			
3	Understand & evaluate the performance of Fuzzy Logic & Systems.			
4	Understand the Genetic Algorithms.			
5	Design & analyze Hybrid Systems.			
6	Understand Soft Computing concepts, technologies, and applications.			
7	Understand the underlying principle of soft computing with its usage in various application.			
Course	Semester	(Open Elective) Graph Theory &	L: 3 T: 0 P: 0 C: 3	
Outcome	III Sem	<b>Optimization Techniques (M20MA02)</b>		
1	Understand the	Understand the various types of graph Algorithms and graph theory properties.		
2	Analyze the NP – complete problems.			
3	Distinguish the features of the various tree and matching algorithms.			
4	Appreciate the applications of digraphs and graph flow.			
5	Understand the	linear programming principles and its conversion.		
6	Design and employ appropriate method for solving computing problems.			



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Course	Semester	(Open Elective) Waste Management	L: 3 T: 0 P: 0 C: 3	
Outcome	III Sem	(M20SE27)		
1	Understand how waste management practices protect environmental health and safety.			
2	Apply physical and chemical analysis on municipal solid wastes.			
3	Enhance the route	for solid waste collection and transport system		
4	Develop a method	to use energy from solid wastes.		
5	Explain different r	nethods of disposal of hazardous solid waste.		
Course	Semester	Dissertation Phase-I (M20VL25)	L: 0 T: 0 P: 20 C:10	
Outcome	III Sem			
After the con	npletion of this co	urse, the students should be able to		
1	In Master's Project Phase-I, the students should select a recent topic from a reputed International Journal, preferably IEEE, ACM, Springer in the field that has direct or indirect relation to the area of specialization.			
2	After conducting a detailed literature survey, they should compare and analyze research work done and review recent developments in the area and prepare an initial design of the work to be carried out as Master's Project			
3	It is mandatory that the students should refer National and International Journals and conference proceedings while selecting a topic for their Project.			
4	Emphasis should be given for introduction to the topic, literature survey, and scope of the proposed work along with some preliminary work carried out on the Project topic.			
5	Students should submit a copy of Phase-I Project report covering the content discussed above and highlighting the features of work to be carried out in Phase-II of the Project.			
Course	Semester	Dissertation Phase-II (M20VL26)	L: 0 T: 0 P: 32 C:16	
Outcome	IV Sem			
After the con	After the completion of this course, the students should be able to			
1	Use specialized knowledge and skills in engineering and apply it effectively on a project.			
2	Apply knowledge of the 'real world' situations that a professional engineer can encounter.			
3	Apply critical and creative thinking in the design of VLSI System Design projects.			
4	Demonstrate a sound technical knowledge of selected project topic.			
5	Demonstrate the skills and attitude of a professional engineer.			
6	Summarize an appropriate list of literature review, analyze previous work and relate them to current project.			
7	Deliver technical seminar based on the Project work carried out.			
8	Publish the conducted research work in a National / International Conference or Journal			